

Communication and Synchronization in Multithreaded Reconfigurable Computing Systems

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UNIVERSITÄT PADERBORN
Die Universität der Informationsgesellschaft

Design of CPU/FPGA Systems

- hardware accelerators typically integrated as slave coprocessors
- hardware/software boundary explicit
- tedious to program
- portability issues

software
application

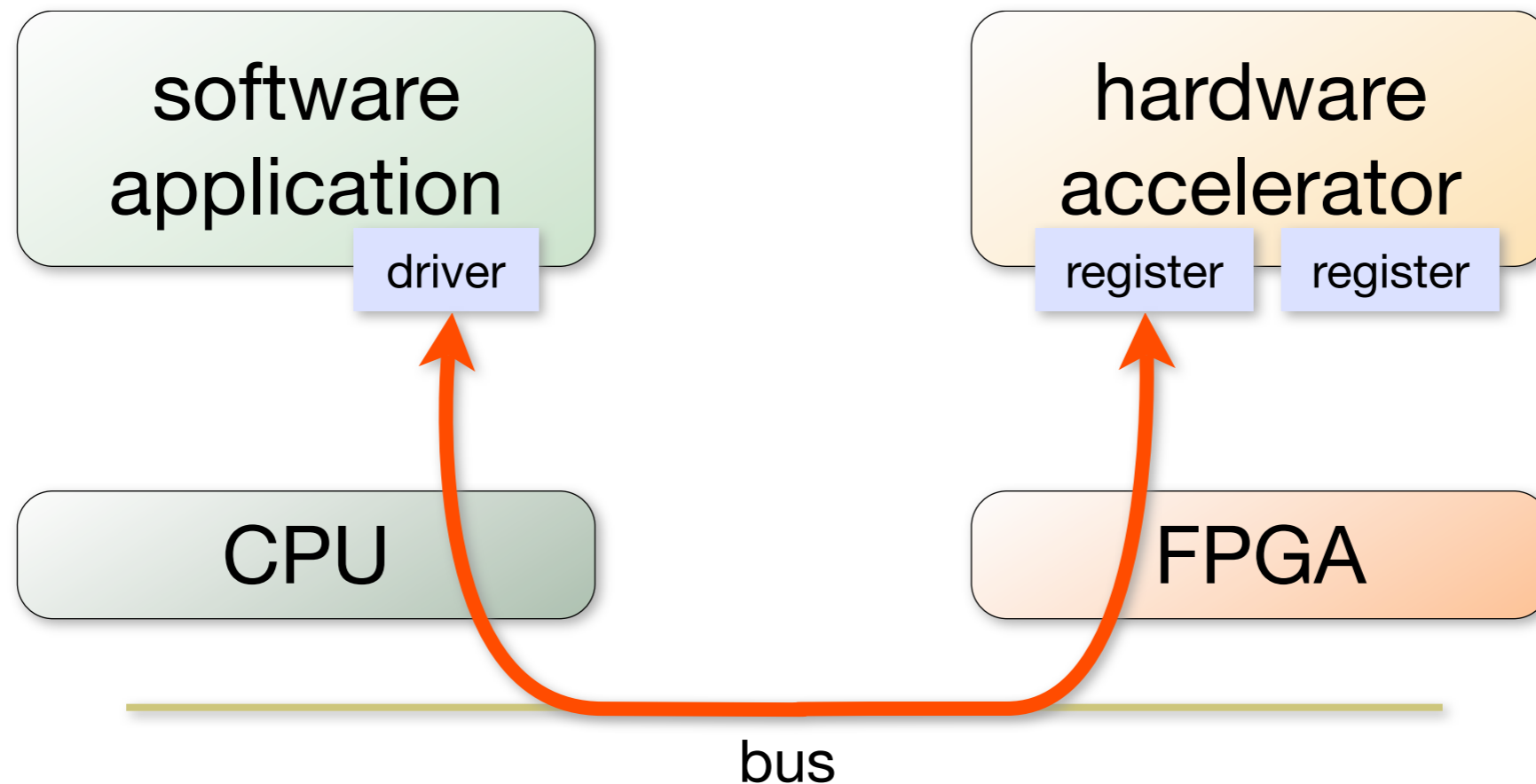
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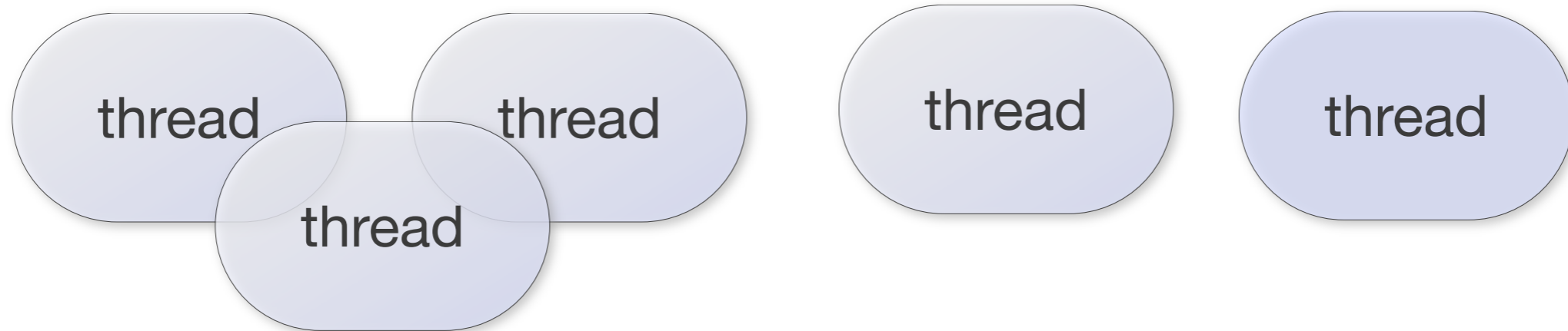


Multithreaded Programming

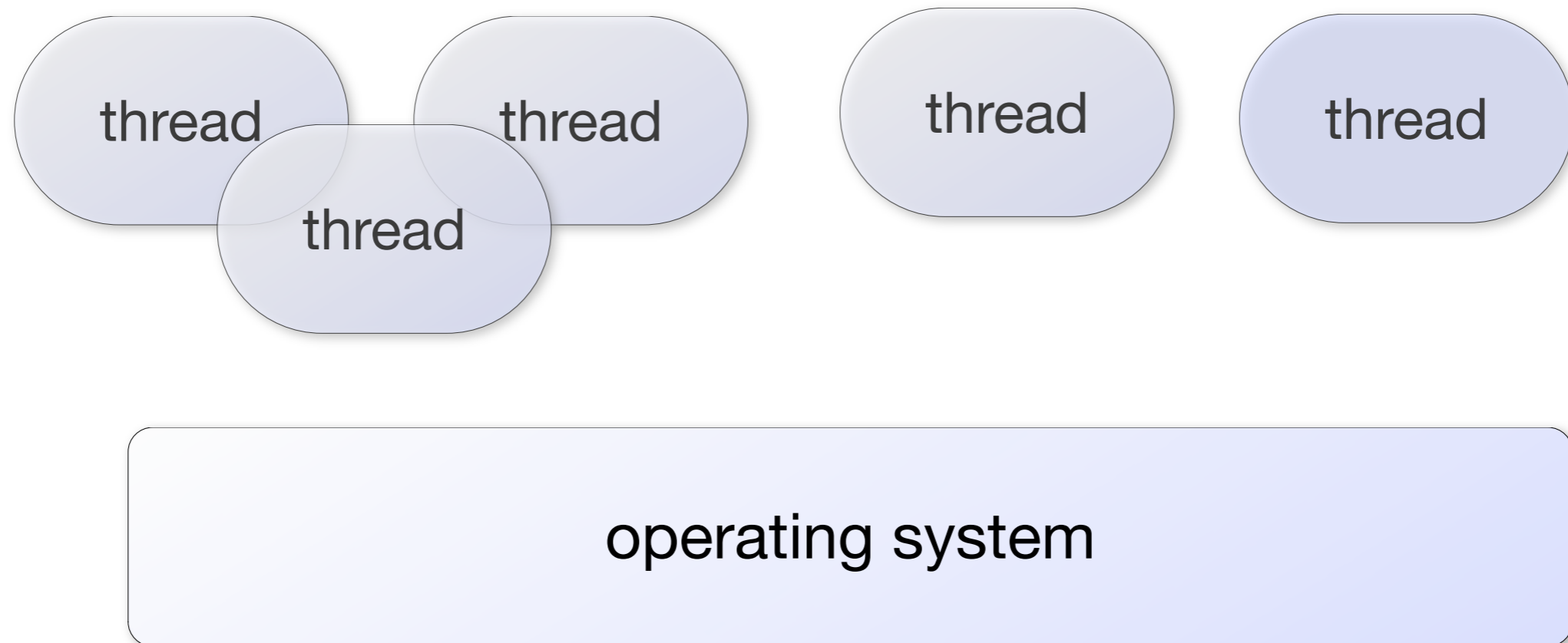


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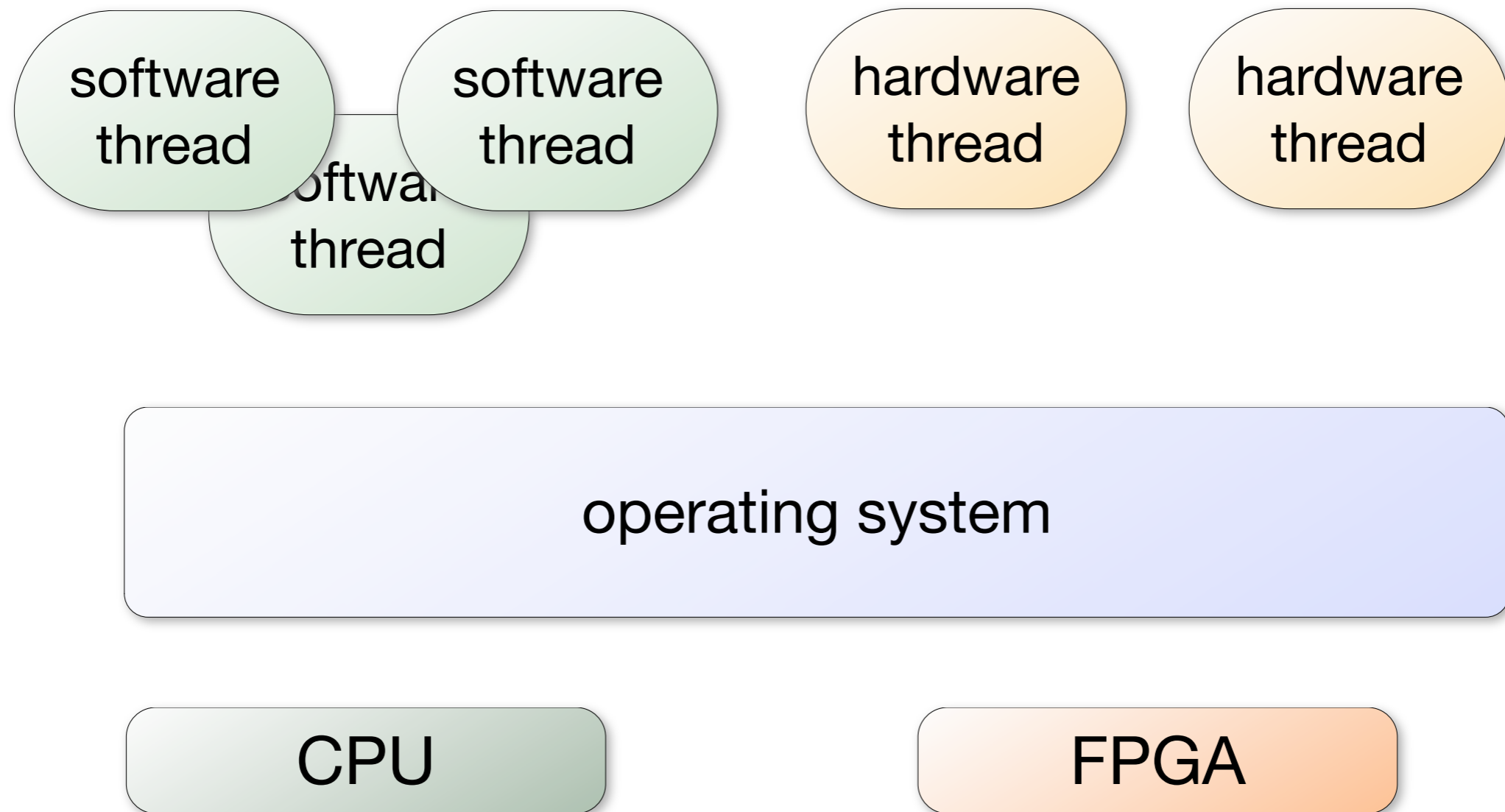
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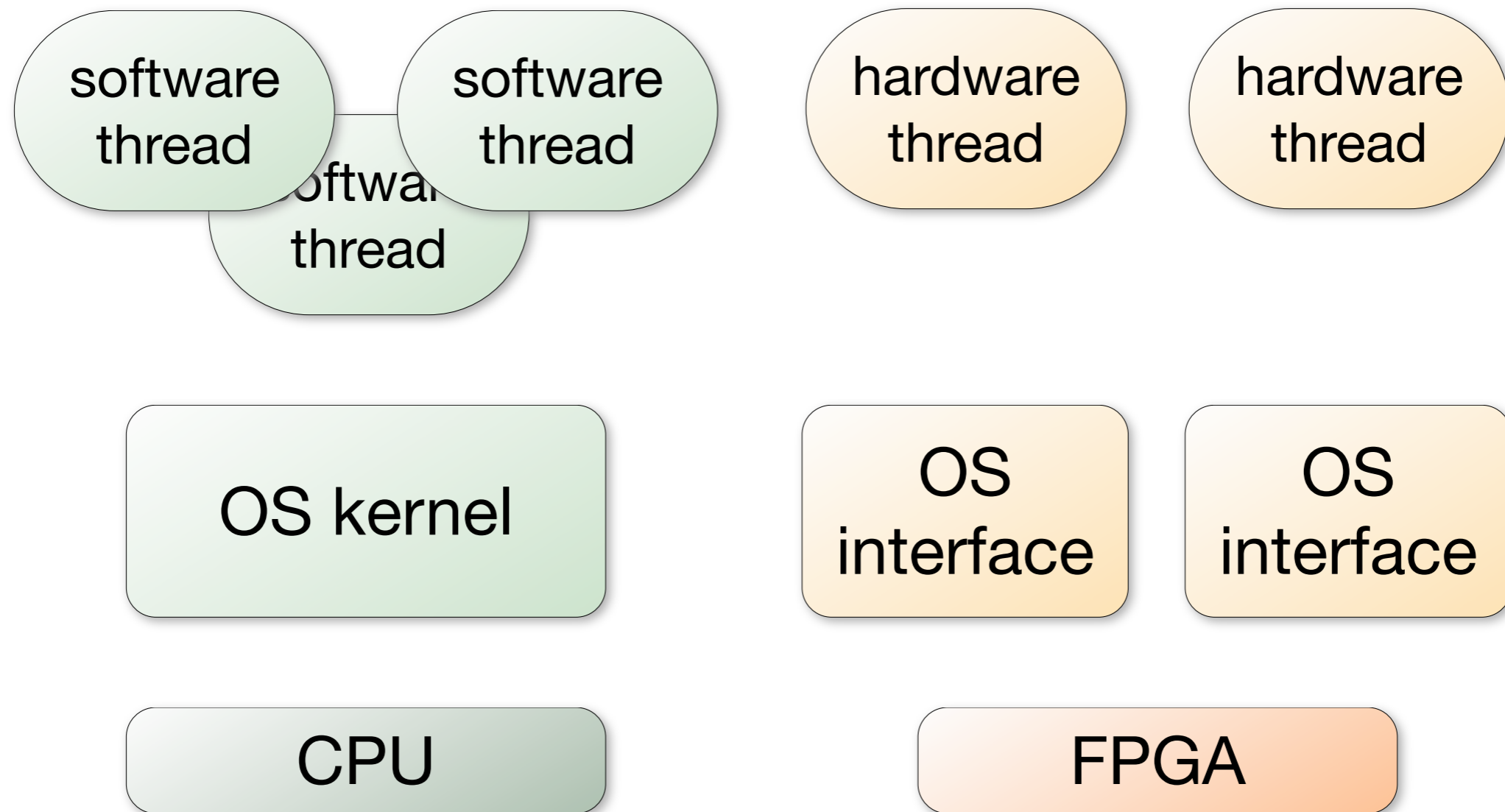
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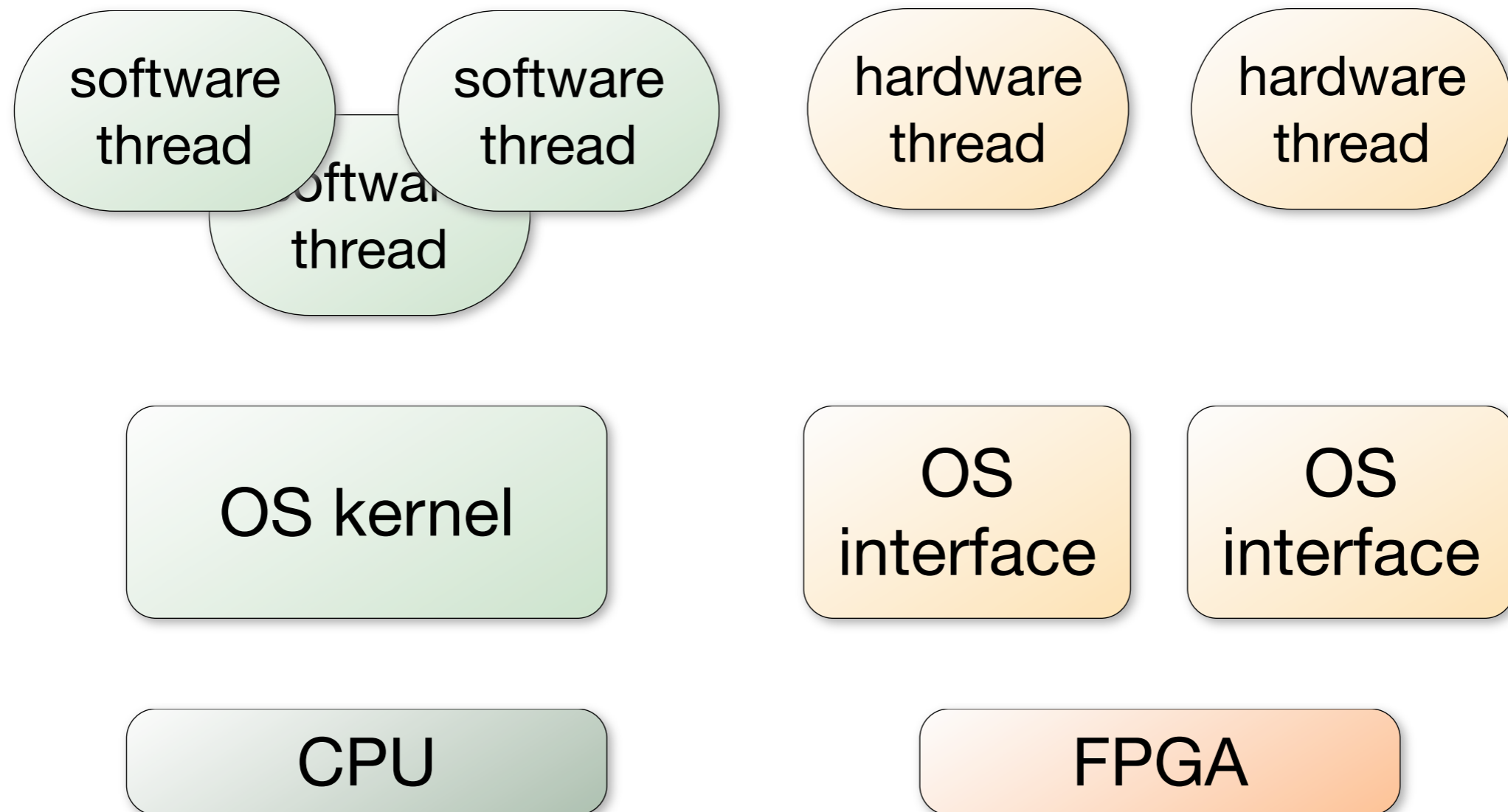
Multithreaded Programming



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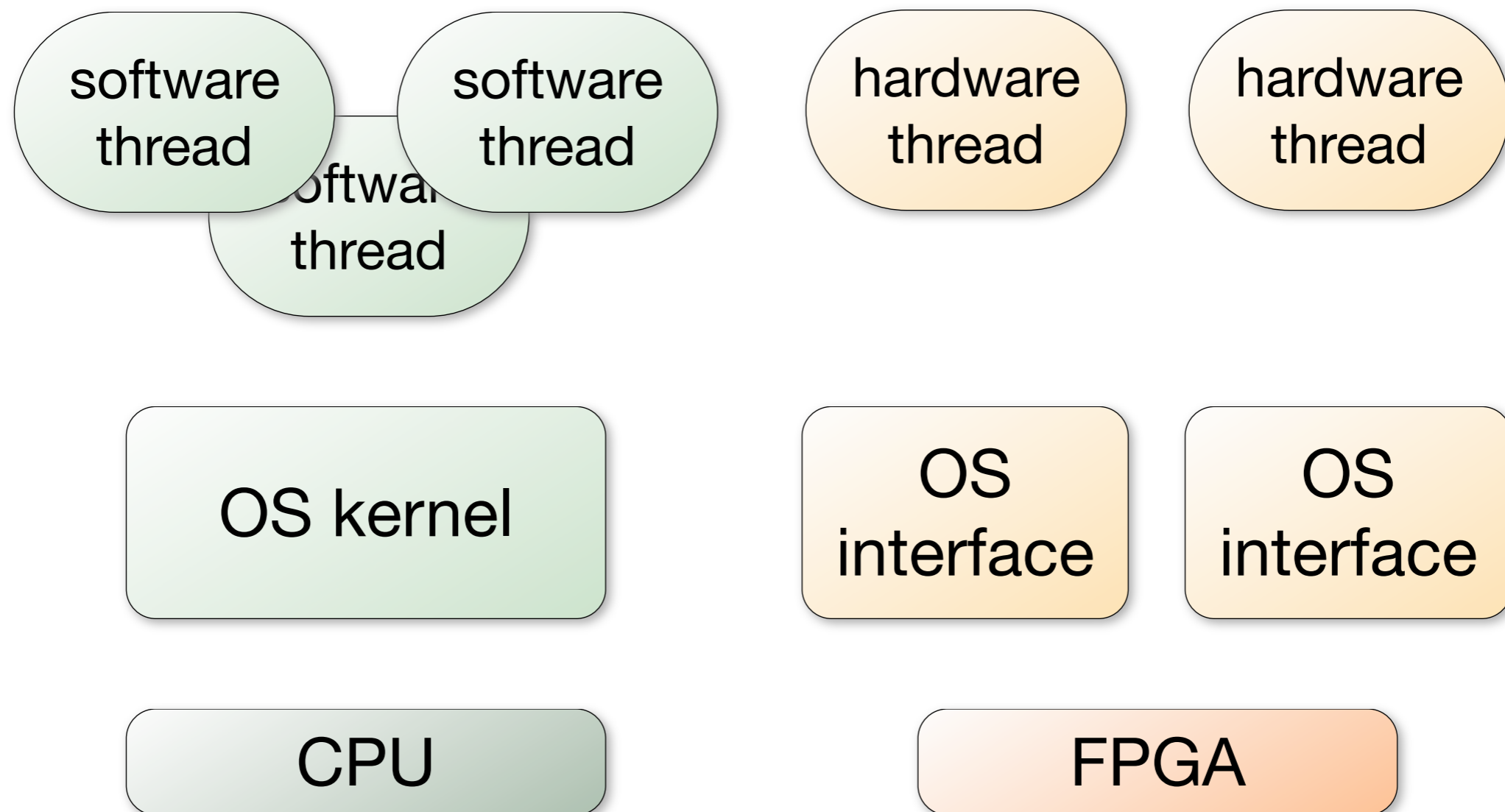


Multithreaded Programming



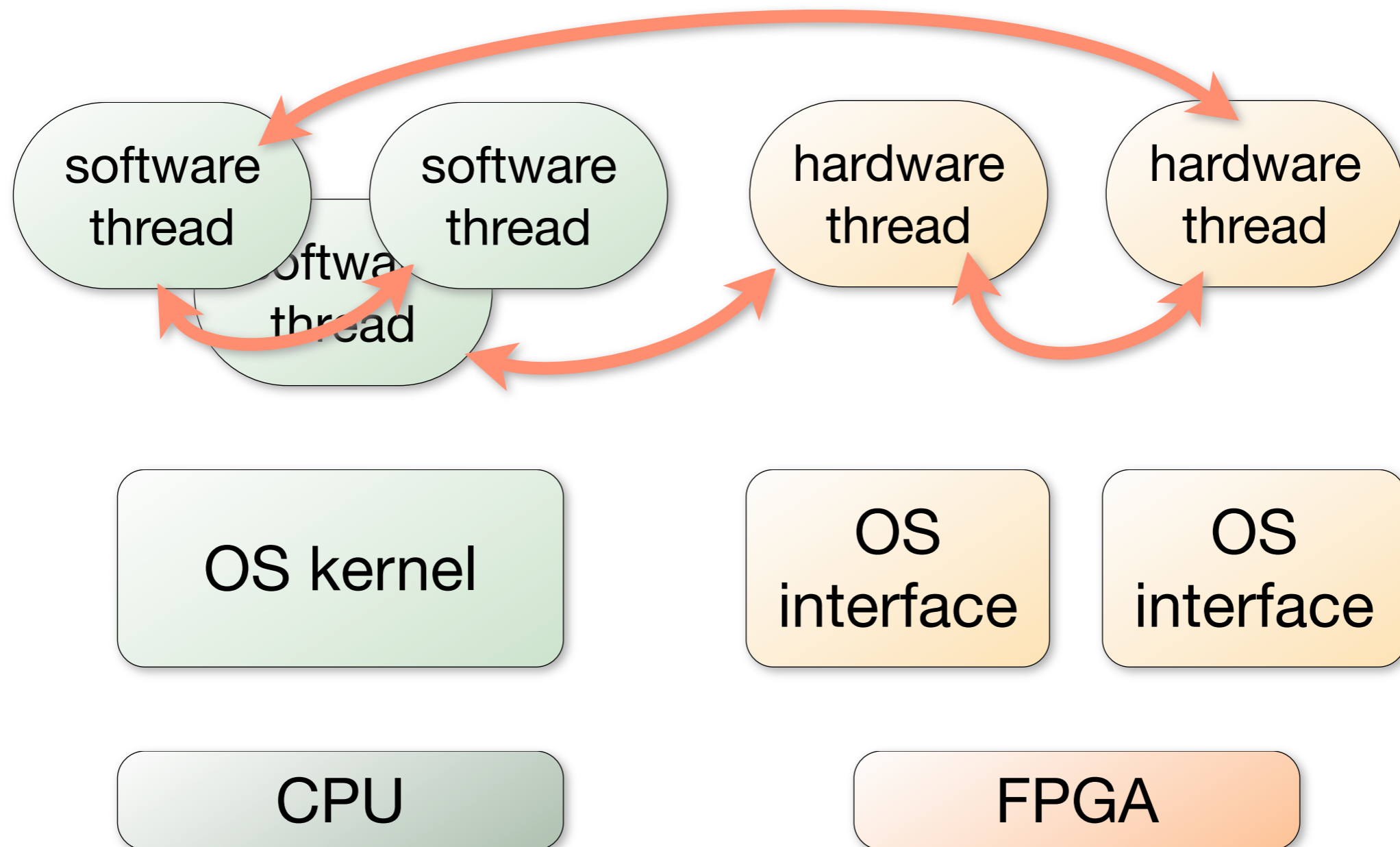
Multithreaded Programming

- communication and synchronization



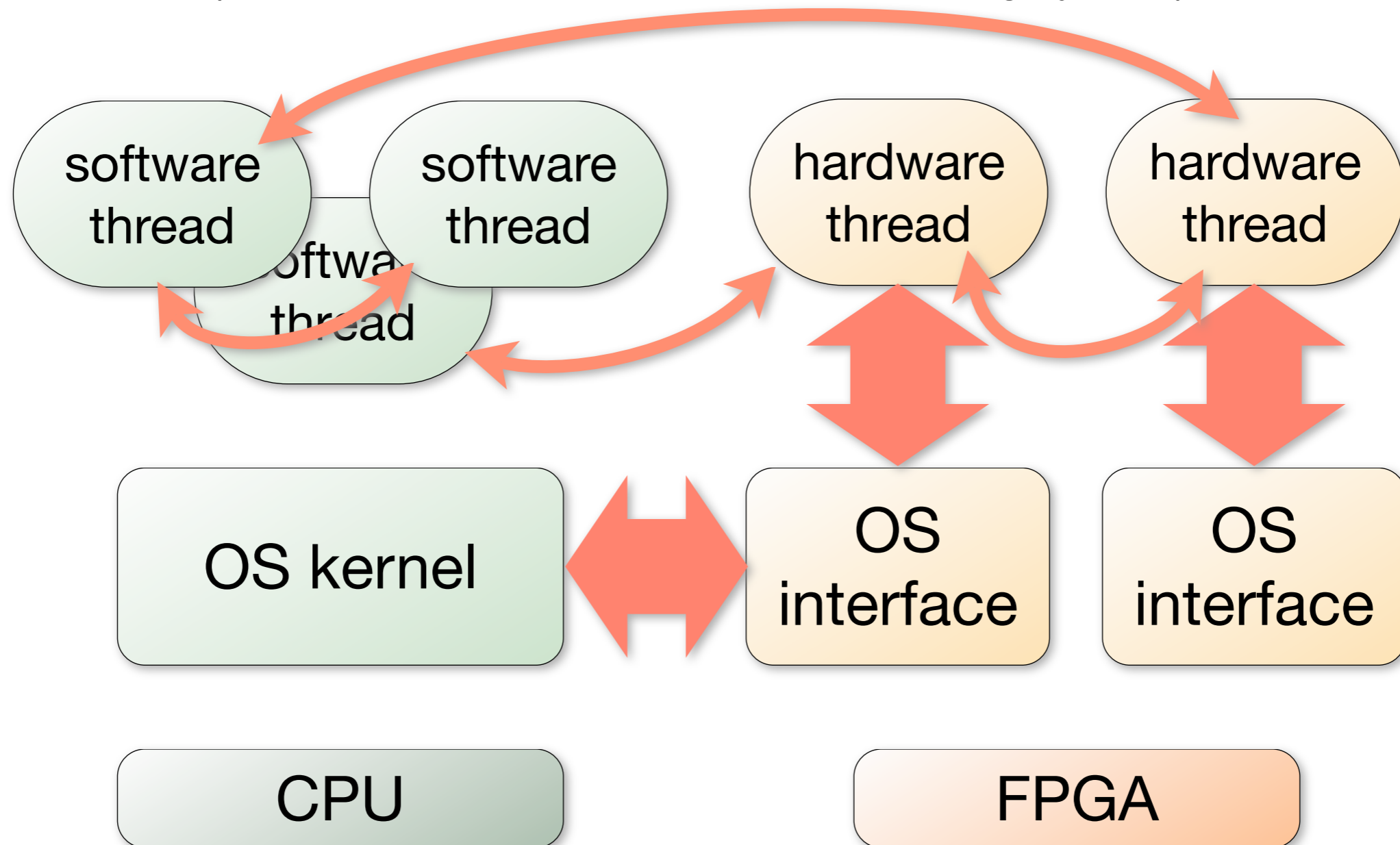
Multithreaded Programming

- communication and synchronization
 - high-level (between the threads themselves)



Multithreaded Programming

- communication and synchronization
 - high-level (between the threads themselves)
 - low-level (between hardware threads and operating system)

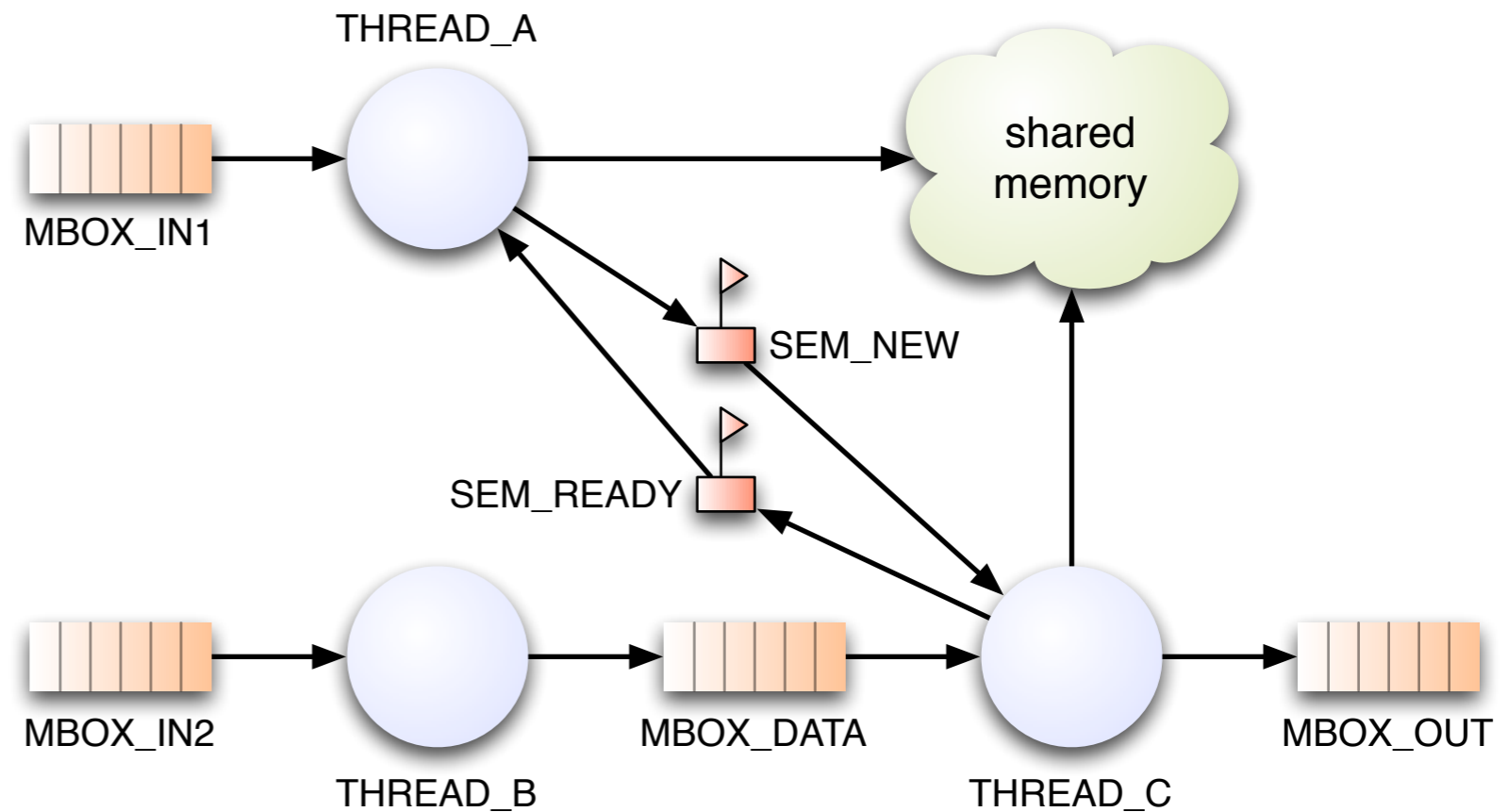


Outline

- motivation
- high-level communication and synchronization
- low-level communication and synchronization
- performance & overheads
- conclusion & outlook

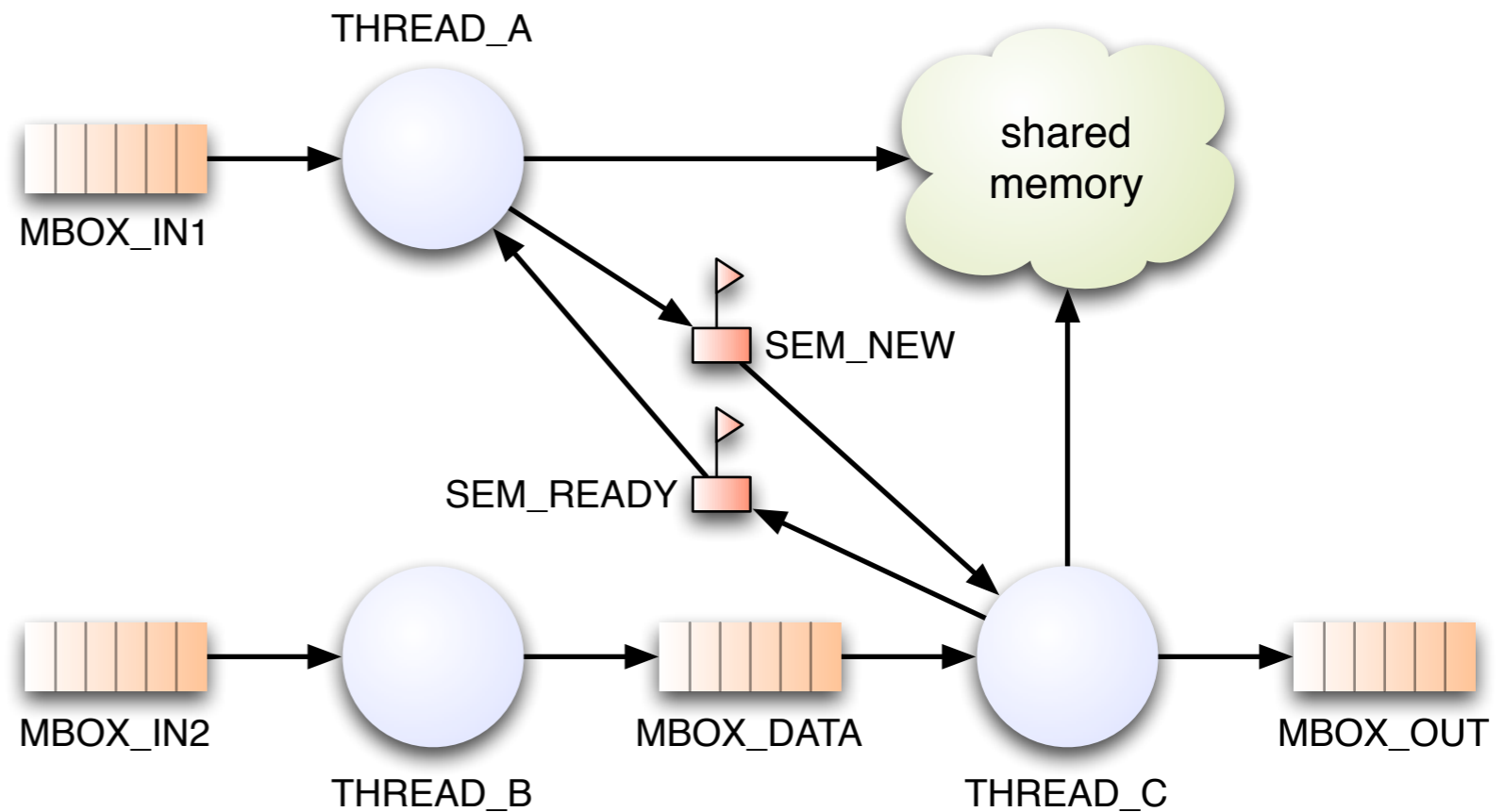
Programming Model

- applications are divided into threads
- threads communicate via operating system objects
 - semaphores
 - mailboxes
 - shared memory
 - ...



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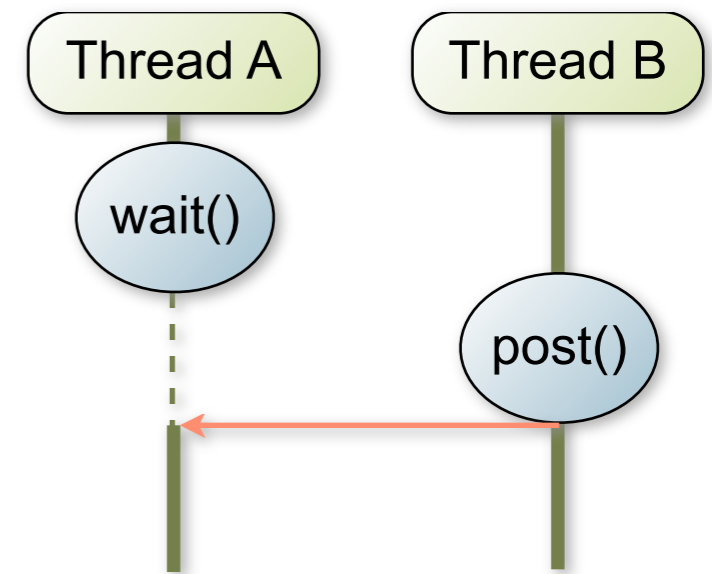
examples for API functions used by threads

software (POSIX, C)	hardware (ReconOS, VHDL)
<code>sem_post()</code>	<code>reconos_sem_post()</code>
<code>pthread_mutex_lock()</code>	<code>reconos_mutex_lock()</code>
<code>mq_send()</code>	<code>reconos_mbox_put()</code>
<code>value = *ptr</code>	<code>reconos_read()</code>
<code>pthread_exit()</code>	<code>reconos_thread_exit()</code>

High-Level Synchronization in ReconOS

■ semaphores

- general mechanism to synchronize execution
- blocking wait() operation, non-blocking post() operation
- supported by **both** hardware and software threads



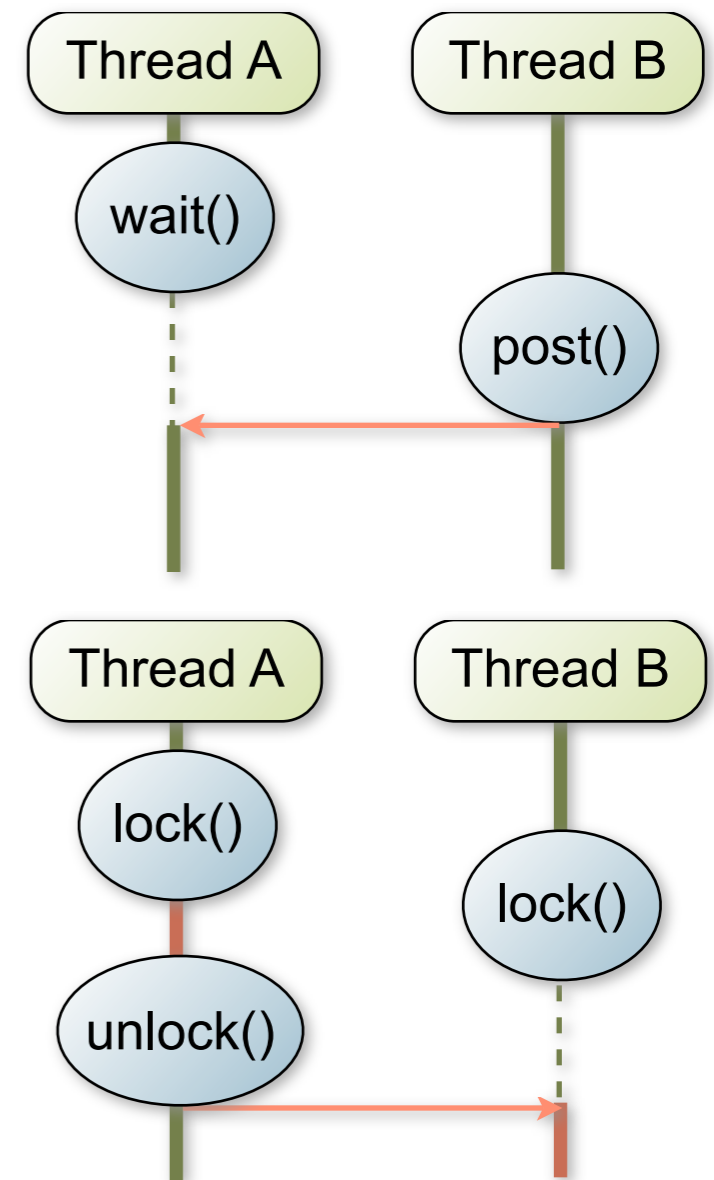
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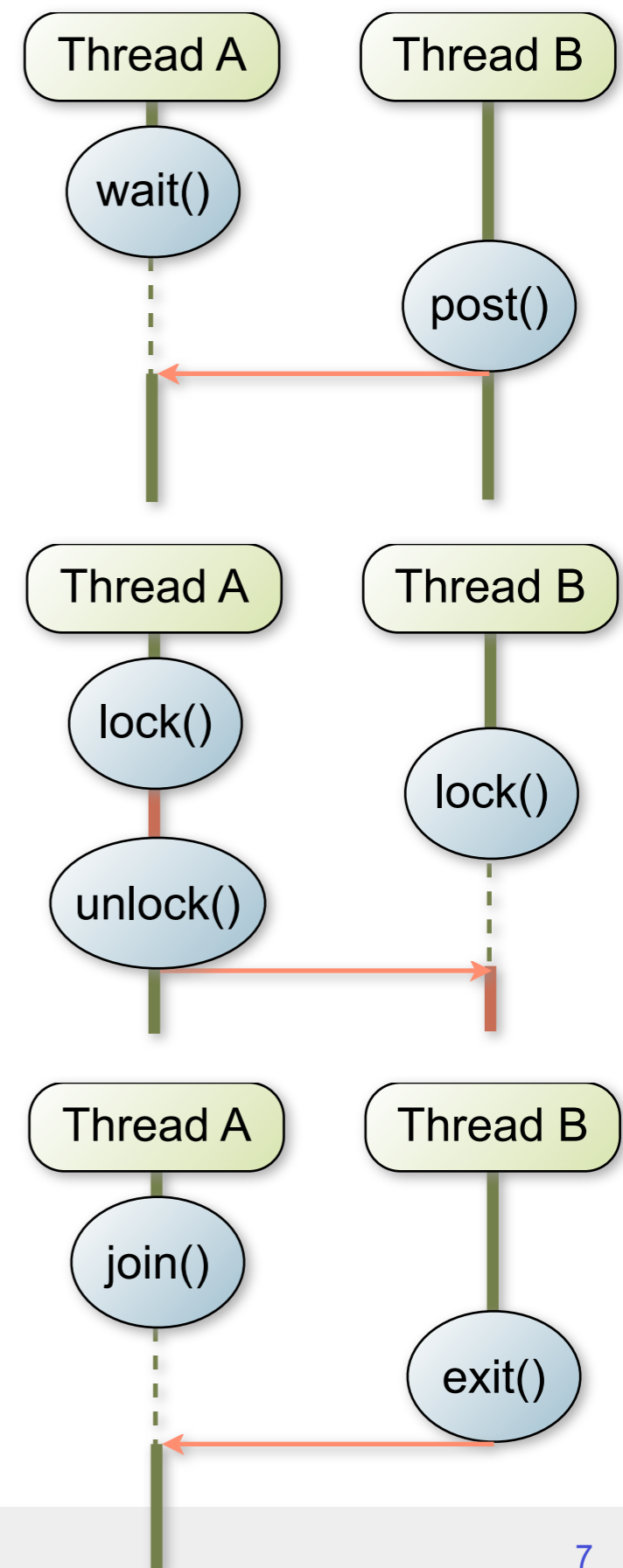
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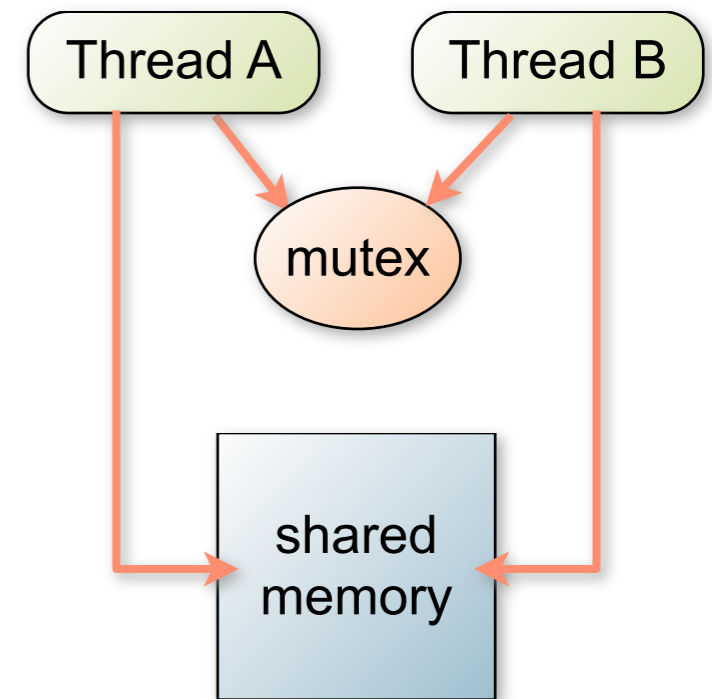
■ thread termination

- a thread can block until another thread exits
- currently, only software threads can join(), but all threads can exit()



High-Level Communication in ReconOS

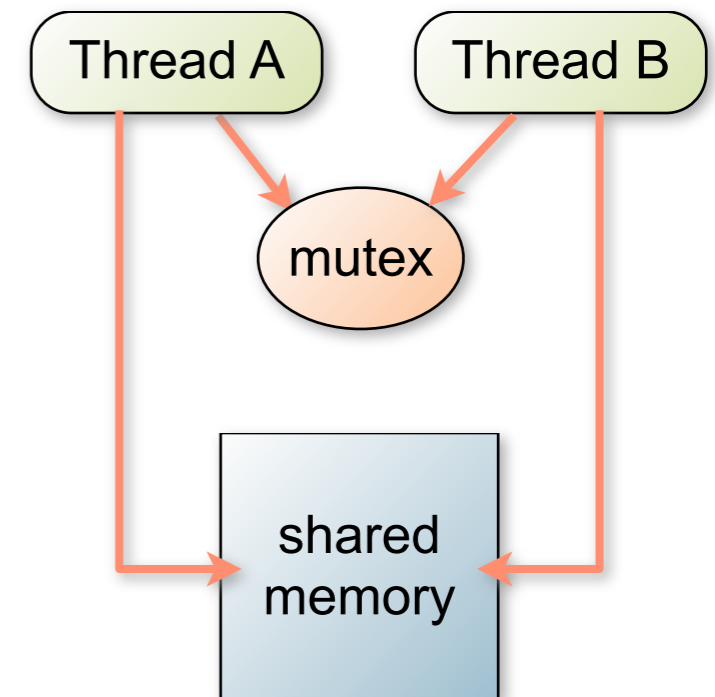
- shared memory
 - all threads have direct access to the entire memory space
 - accesses need to be synchronized using semaphores or mutexes
 - dedicated hardware support for burst transfers



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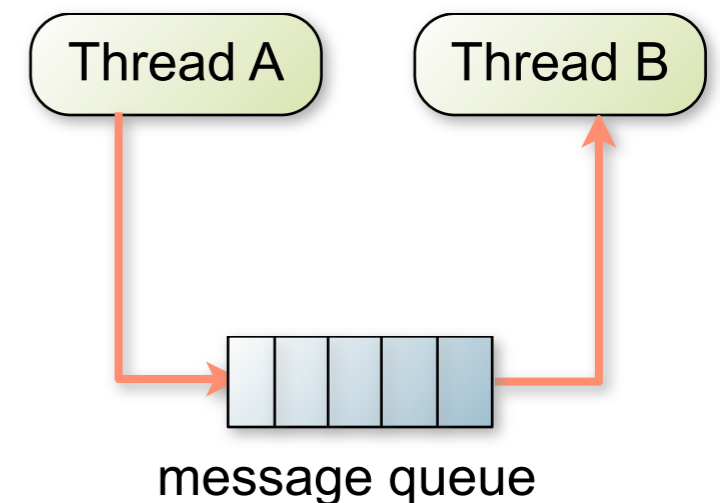
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■ message queues

- can block if queue is empty / full
- combined communication and synchronization primitive
- supported by both hardware and software threads
- dedicated hardware FIFOs for hardware threads

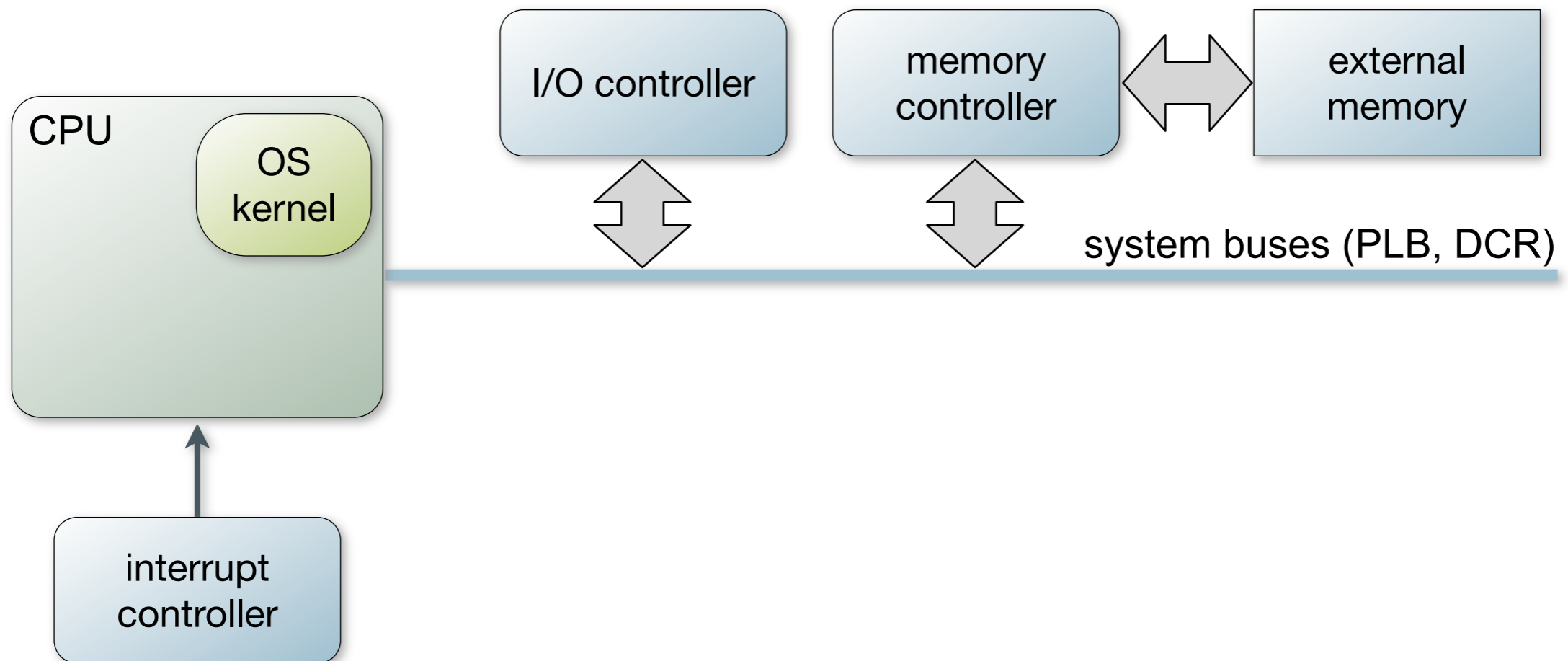


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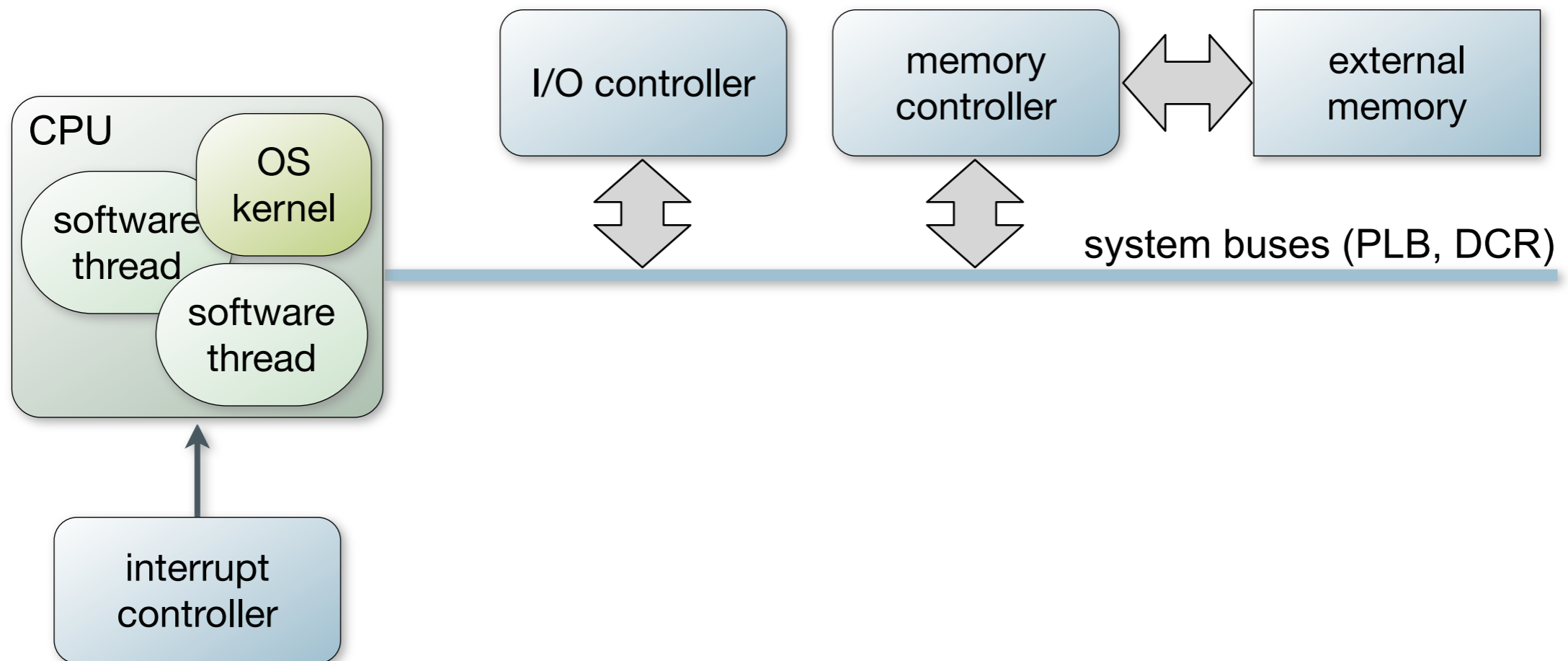
Hardware Architecture

- developed on Xilinx Virtex-II Pro, Virtex-4 FX FPGAs
- based on CoreConnect bus topology
- OS kernel is eCos for PowerPC ported to Virtex



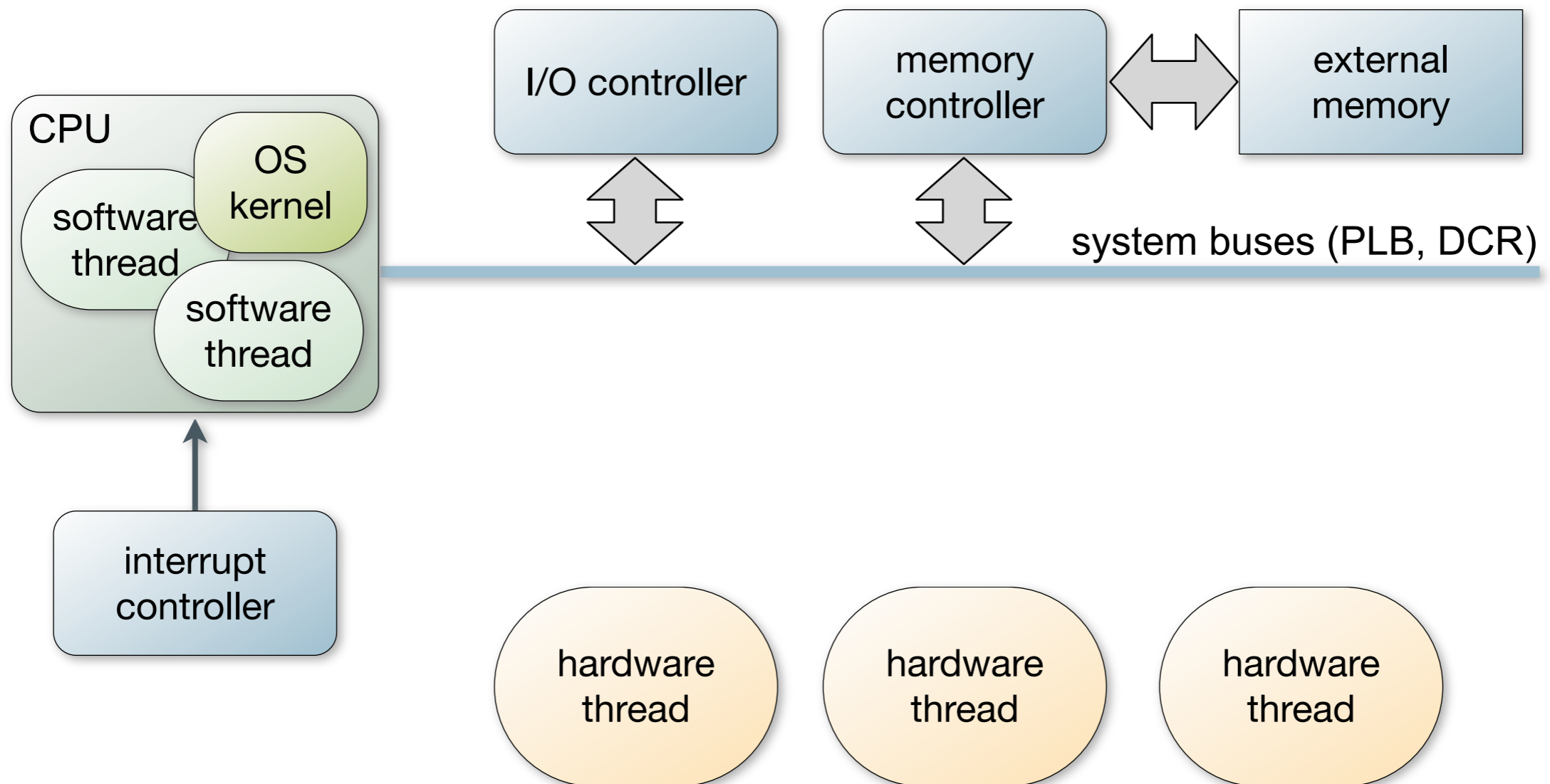
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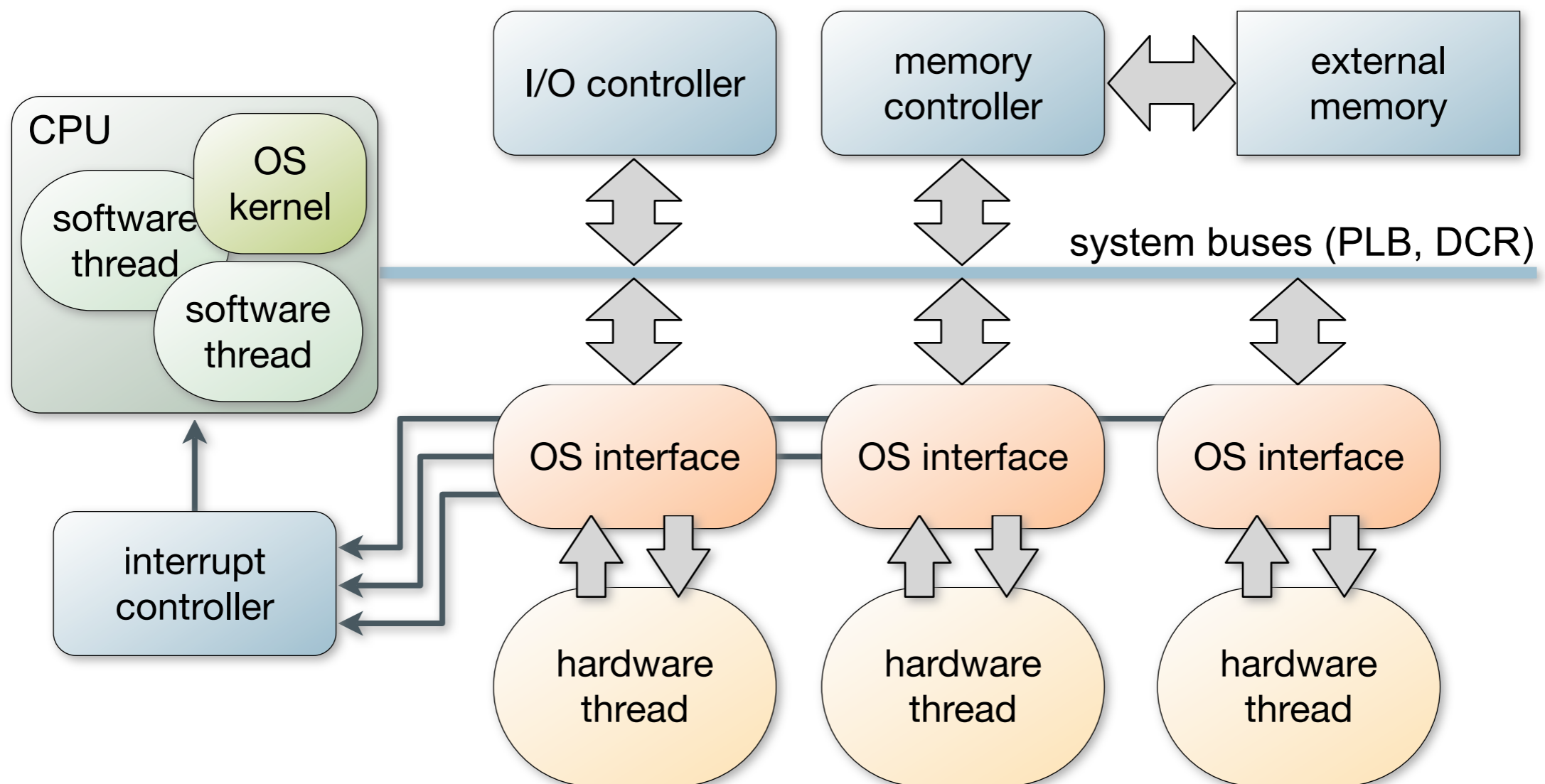
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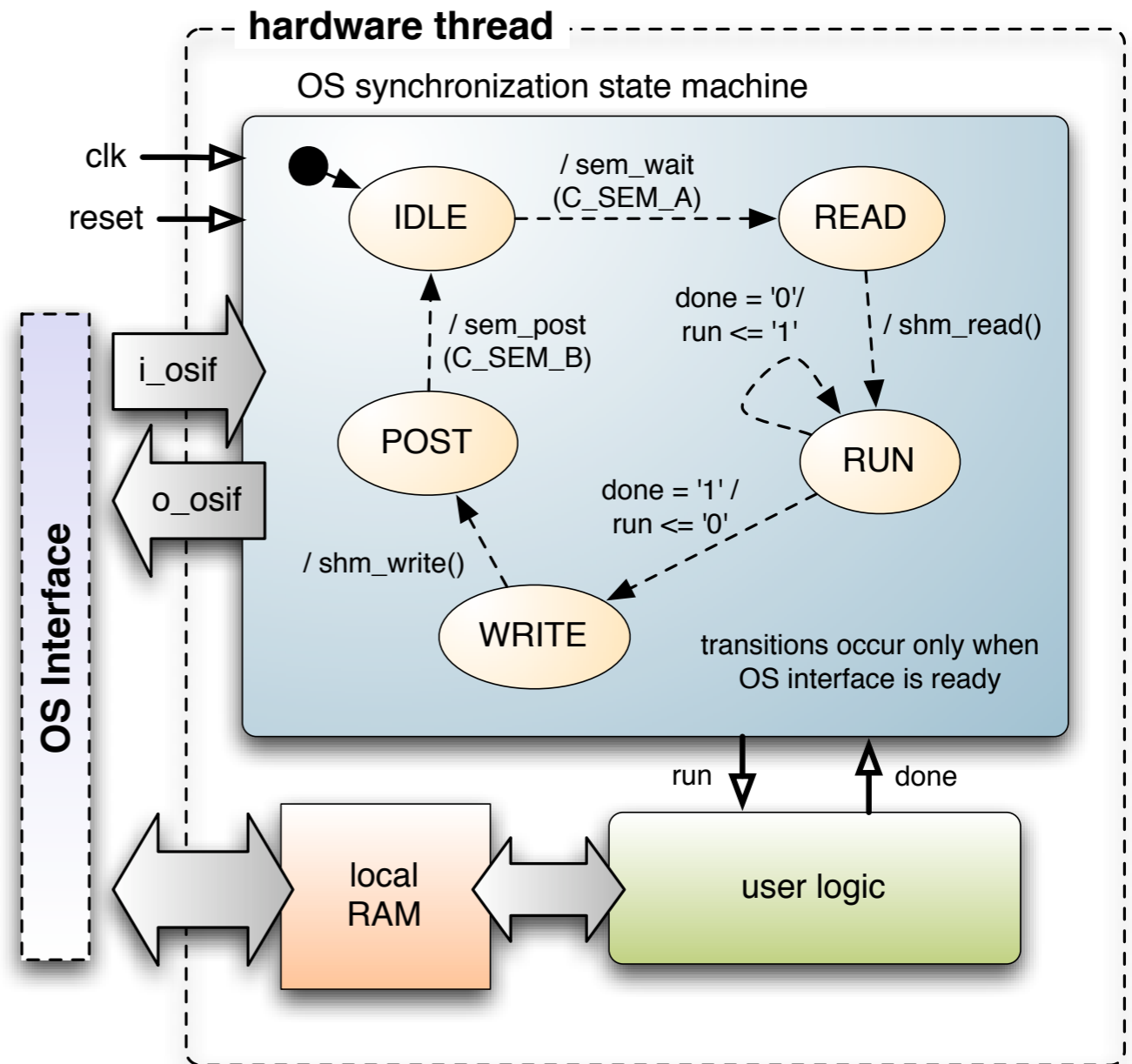


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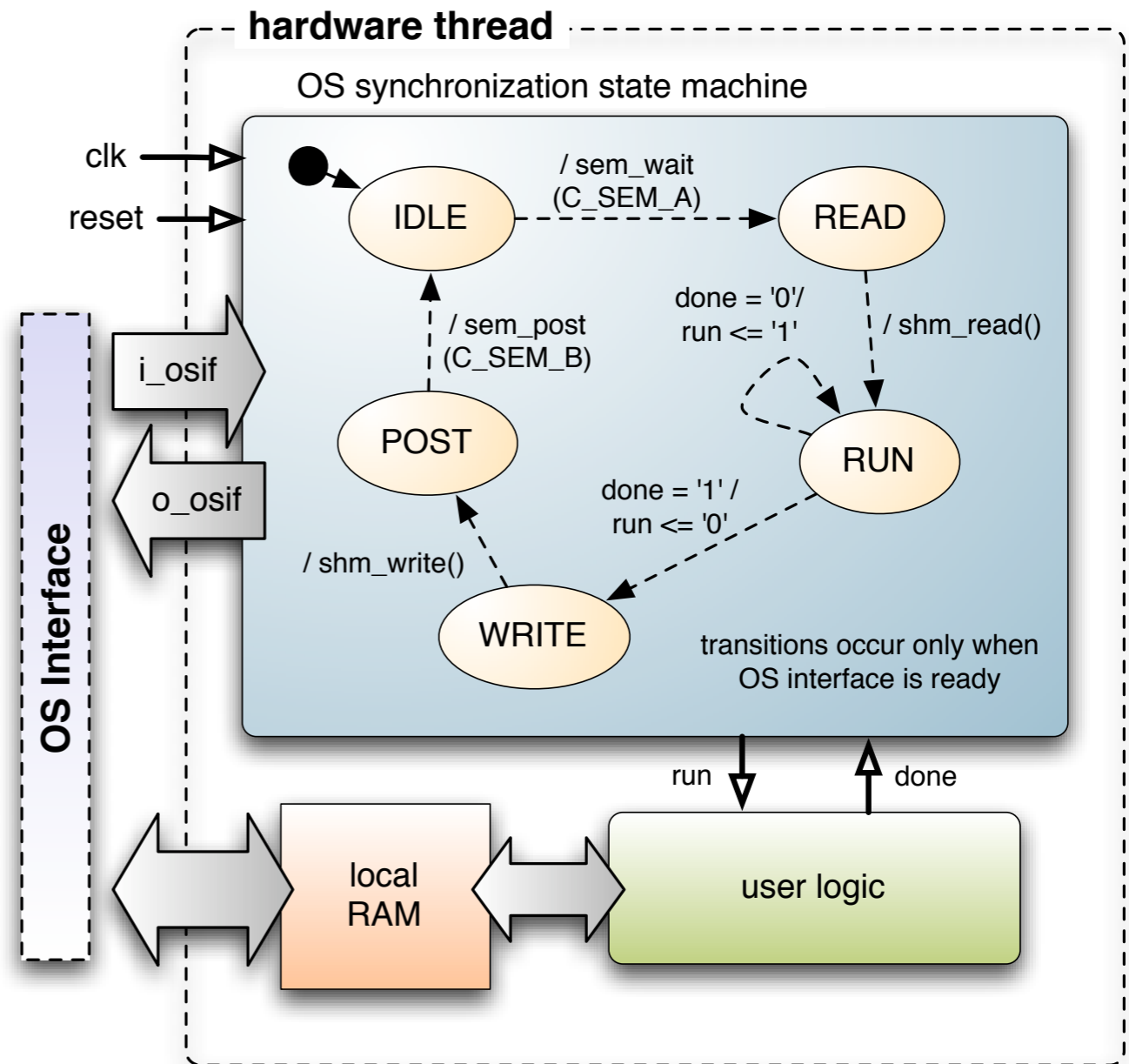


Hardware Thread



Hardware Thread

- a hardware thread consists of two parts

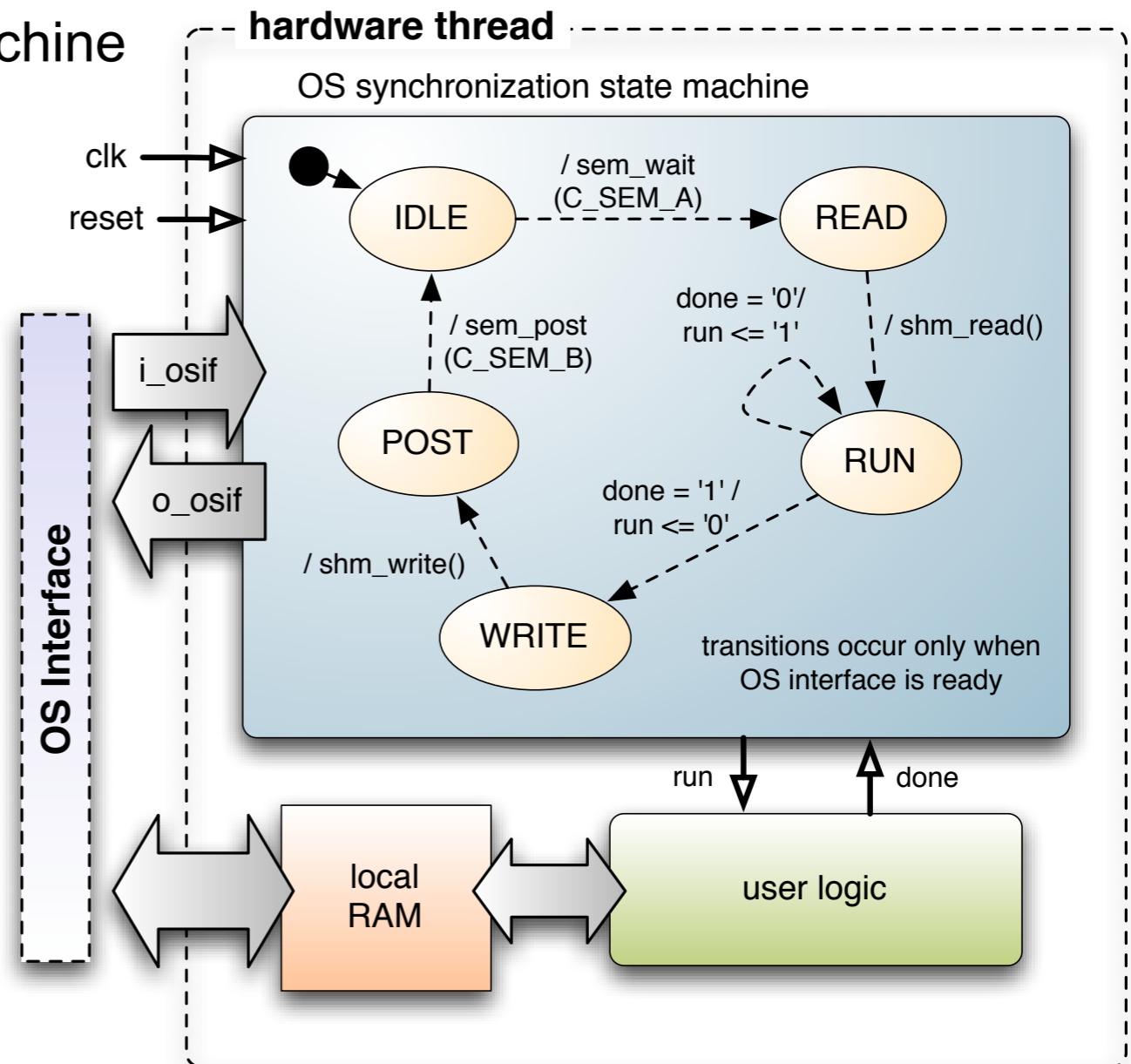


Hardware Thread

- a hardware thread consists of two parts

- an OS synchronization state machine

- synchronizes thread with operating system calls
- serializes access to OS objects via the OS interface
- can be blocked by the OS interface



Hardware Thread

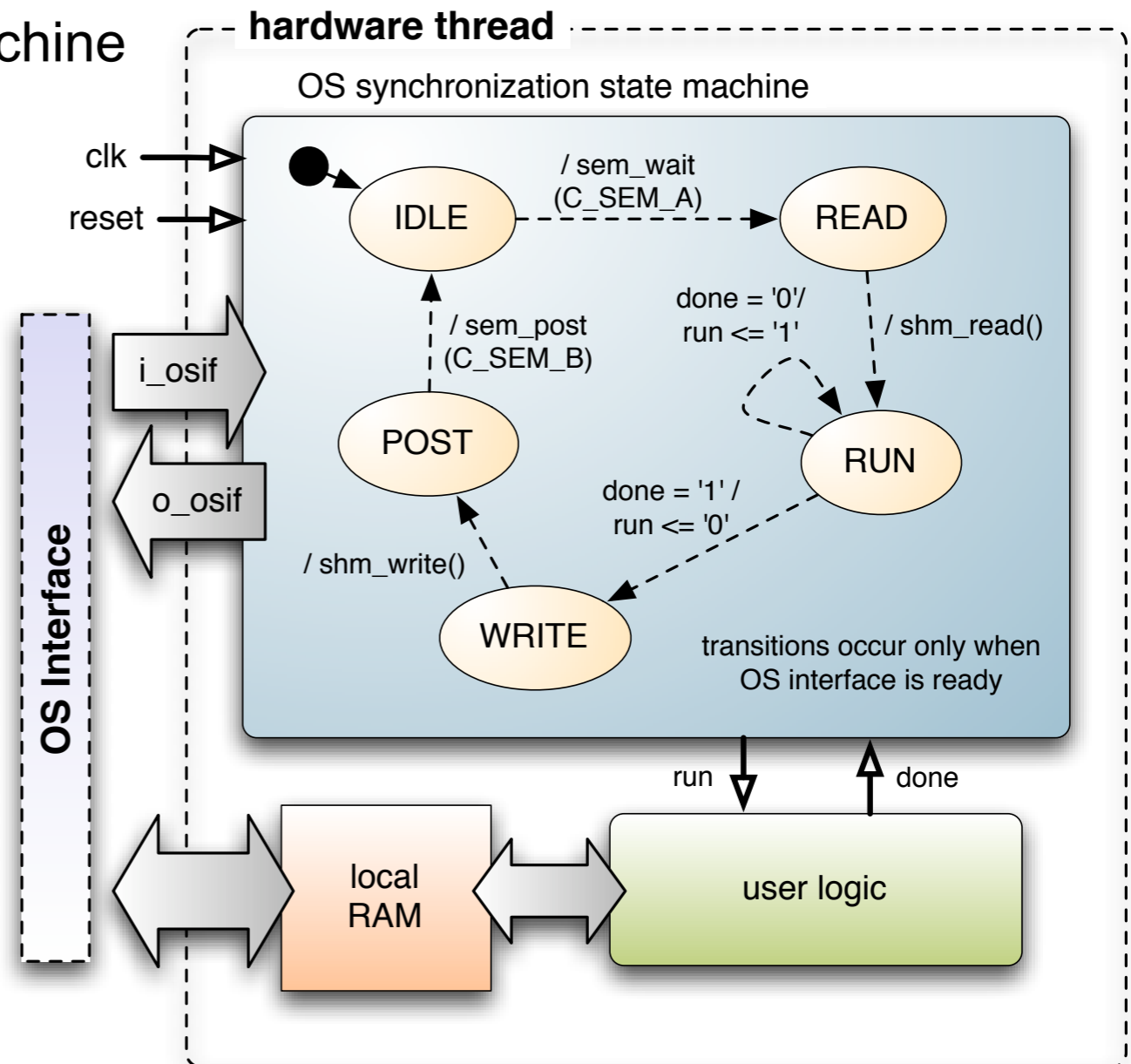
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- parallel “user processes”

- communicate with OS synchronization state machine
- can directly access local memory blocks
- are not necessarily blocked



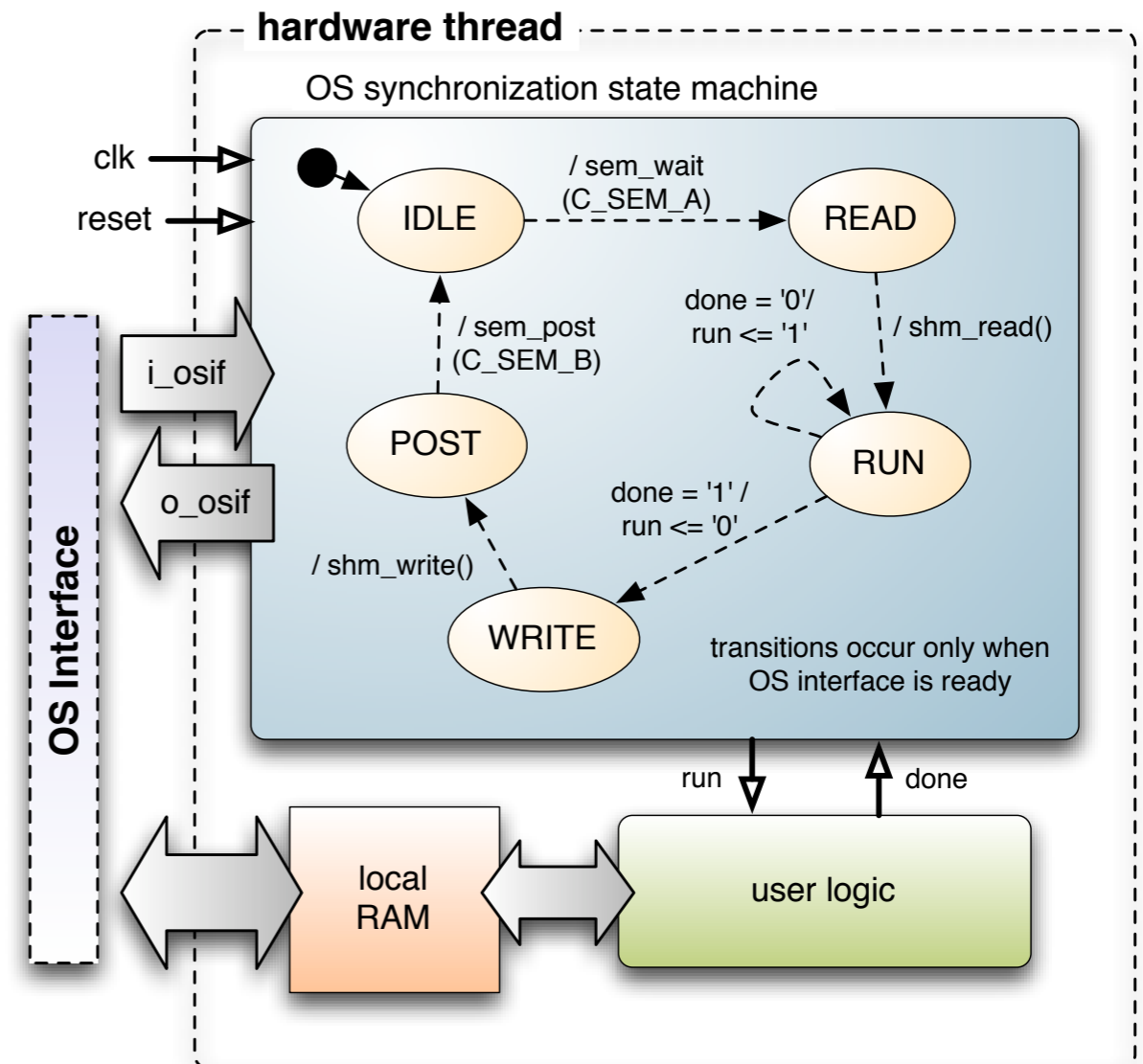
ReconOS API for Hardware Threads

```

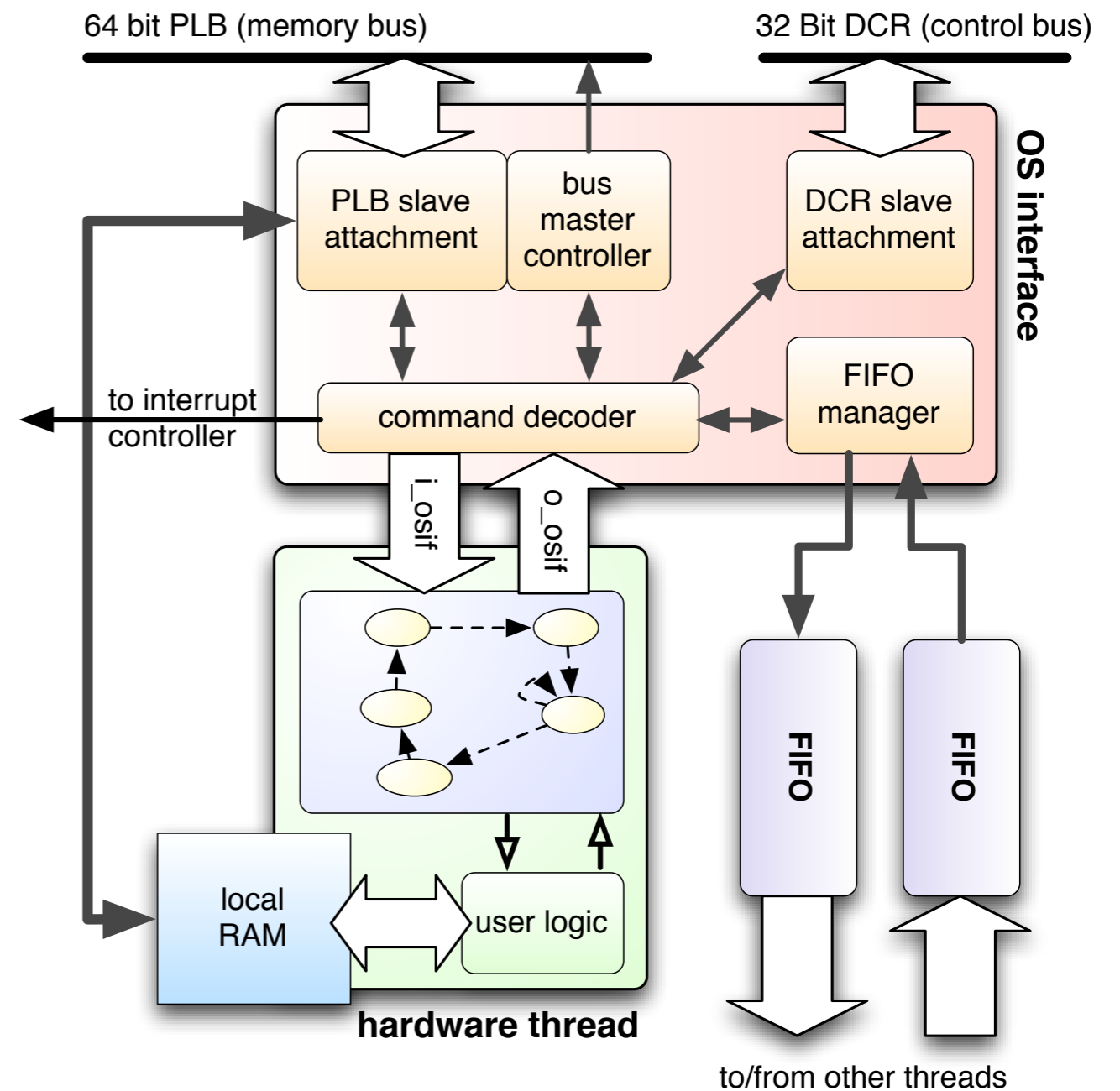
1  osif_fsm: process(clk, reset)
2  begin
3    if (reset = '1') then
4      state <= IDLE;
5      run <= '0';
6      reconos_reset(o_osif, i_osif);
7    elsif rising_edge(clk) then
8      reconos_begin(o_osif, i_osif);
9      if reconos_ready(i_osif) then
10     case state is
11     when IDLE =>
12       reconos_sem_wait(o_osif, i_osif, C_SEM_A);
13       state <= READ;
14
15     when READ =>
16       reconos_shm_read_burst(o_osif, i_osif,
17         local_address,
18         global_address);
19
20       state <= RUN;
21
22     when RUN =>
23       run <= '1';
24       if done = '1' then
25         run <= '0';
26         state <= WRITE;
27       end if;
28
29     when WRITE =>
30       reconos_shm_write_burst(o_osif, i_osif,
31         local_address,
32         global_address);
33
34       state <= POST;
35
36     when POST =>
37       reconos_sem_post(o_osif, i_osif, C_SEM_B);
38       state <= IDLE;
39
40     when others => null;
41   end case;
42 end if;
43 end if;
44 end process;

```

- VHDL function library
- used similar to software API
- may only be used inside OS synchronization state machine

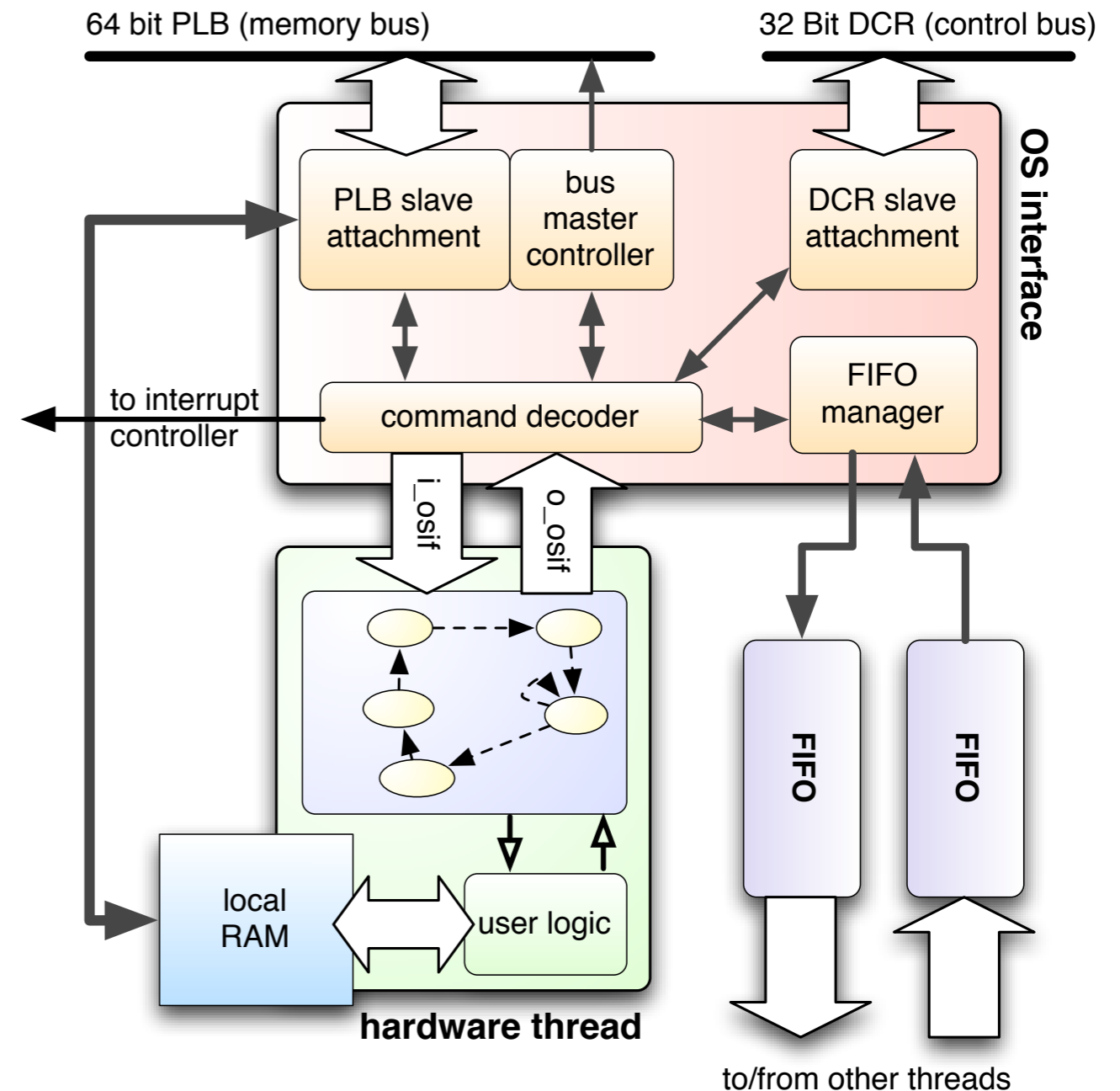


OS Interface



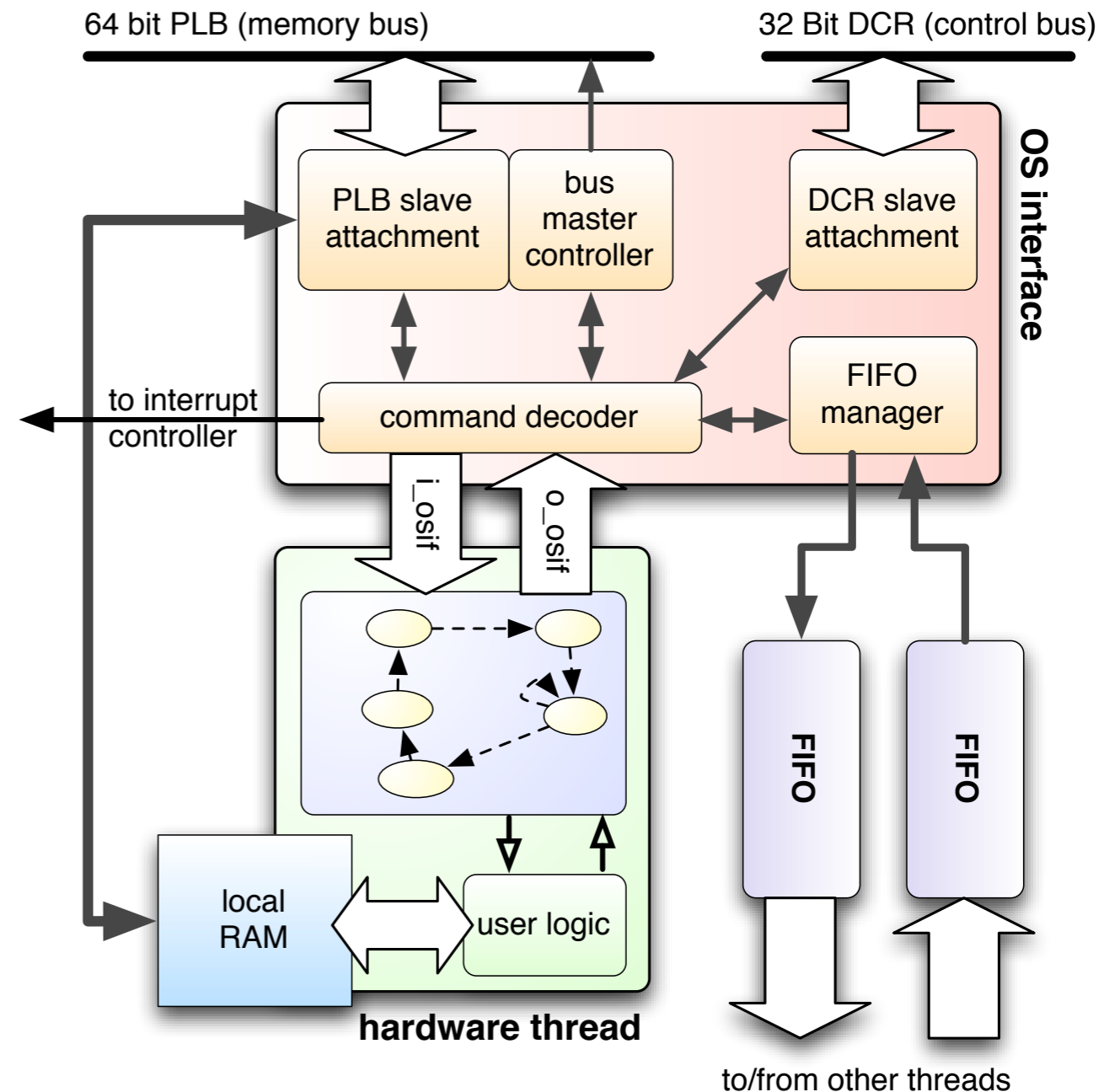
OS Interface

- processes requests from hardware thread
 - handles blocking and resuming of hardware thread



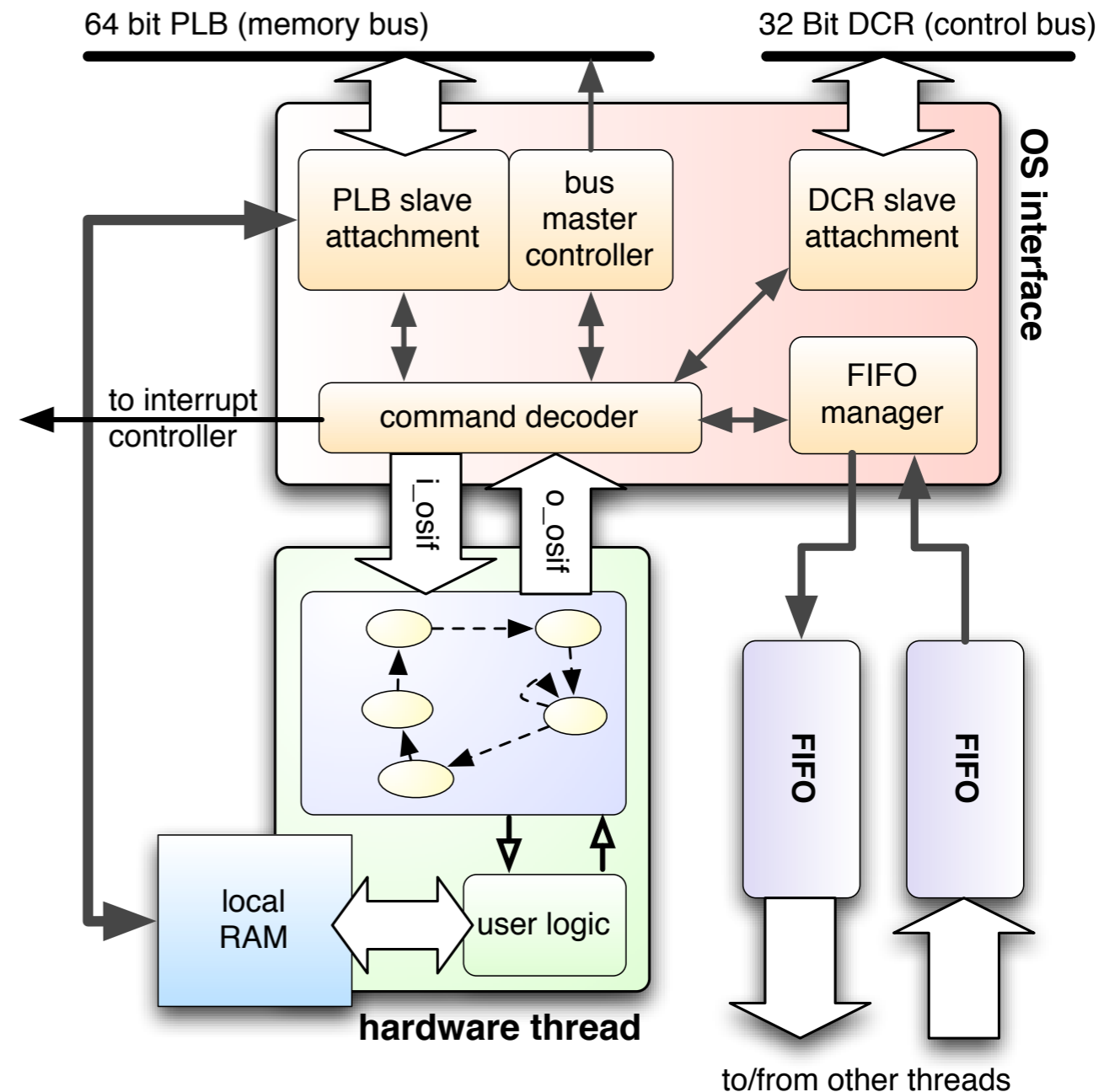
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- relays OS object interactions to CPU
 - DCR interface with bus-addressable registers
 - dedicated interrupt



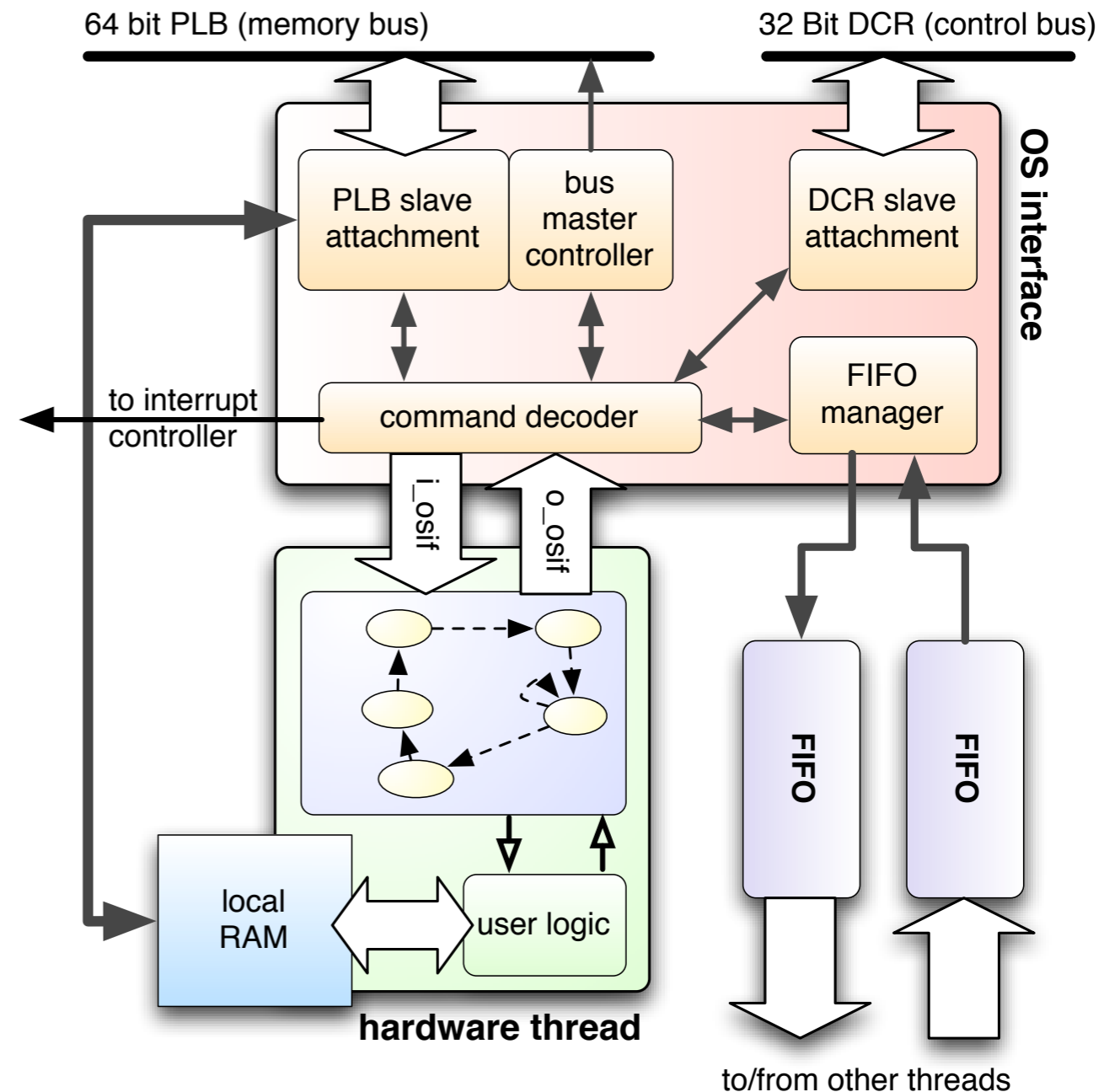
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 - PLB master interface
 - direct access to entire system's address space (memory and peripherals)

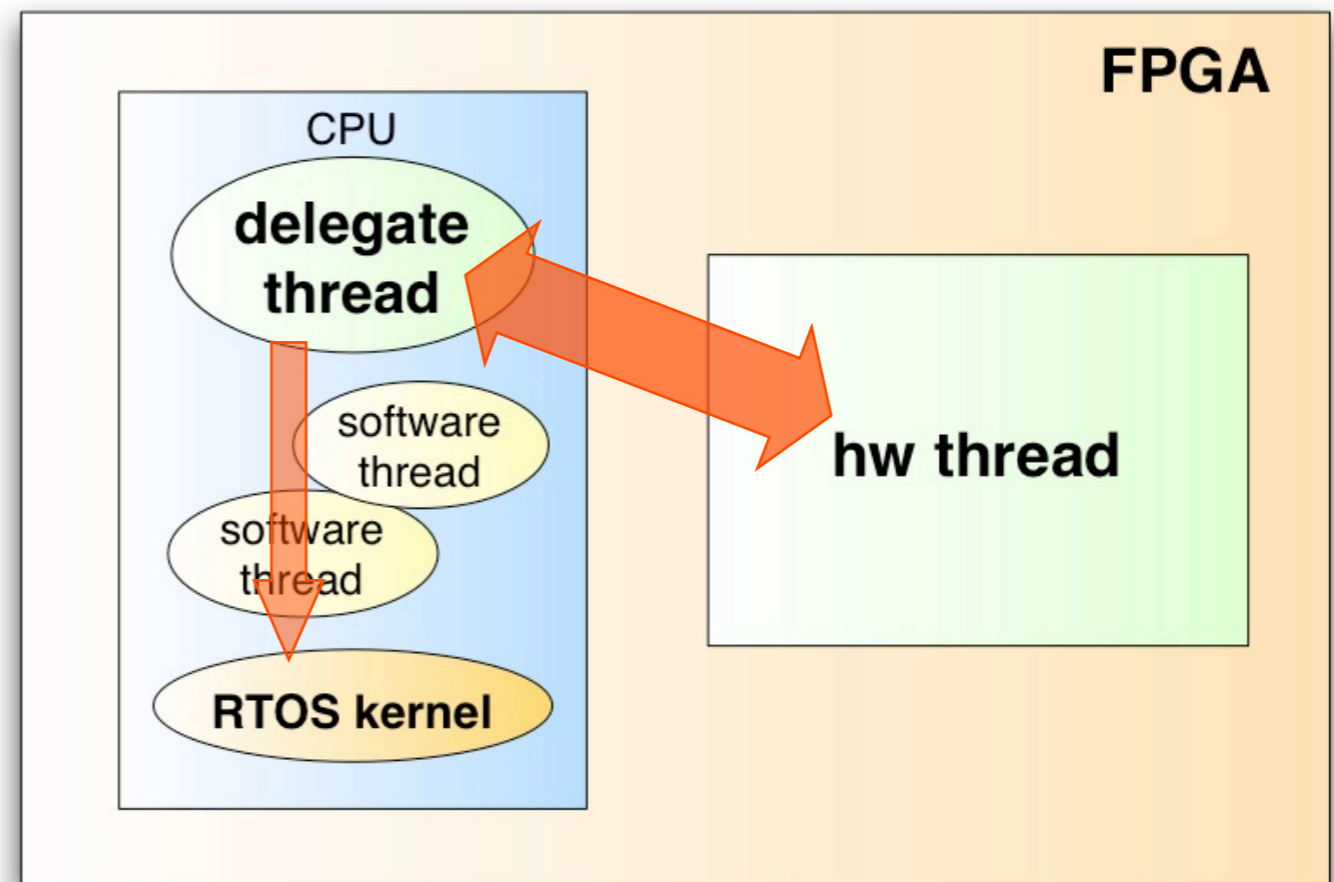


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 - direct access to entire system's address space (memory and peripherals)
- dedicated FIFO channels
 - provide high-throughput hardware support for message passing



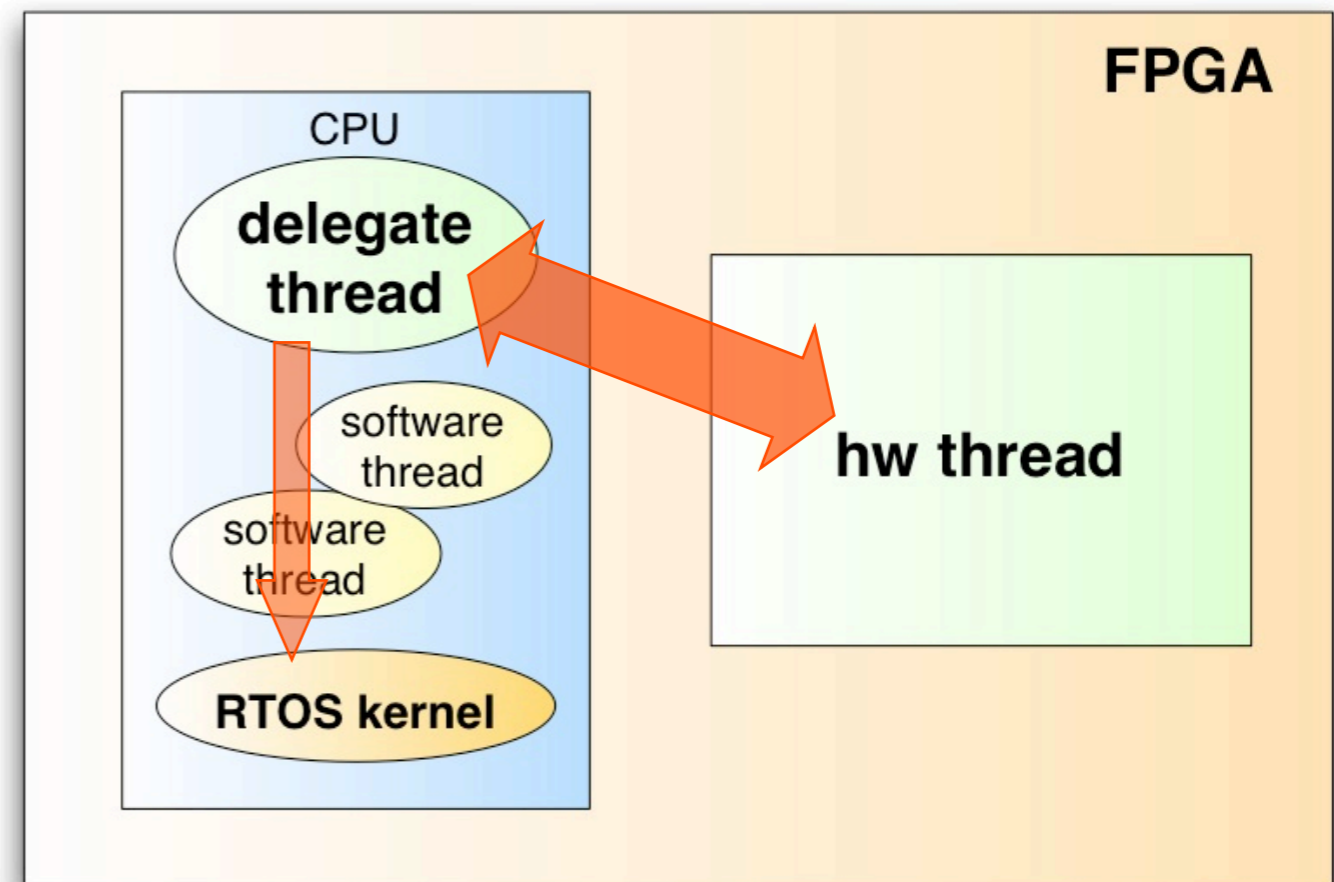
Delegate Threads



Delegate Threads

■ basic mechanism

- a delegate thread in software is associated with every hardware thread
- the delegate thread calls the OS kernel on behalf of the hardware thread
- all kernel responses are relayed back to the hardware thread



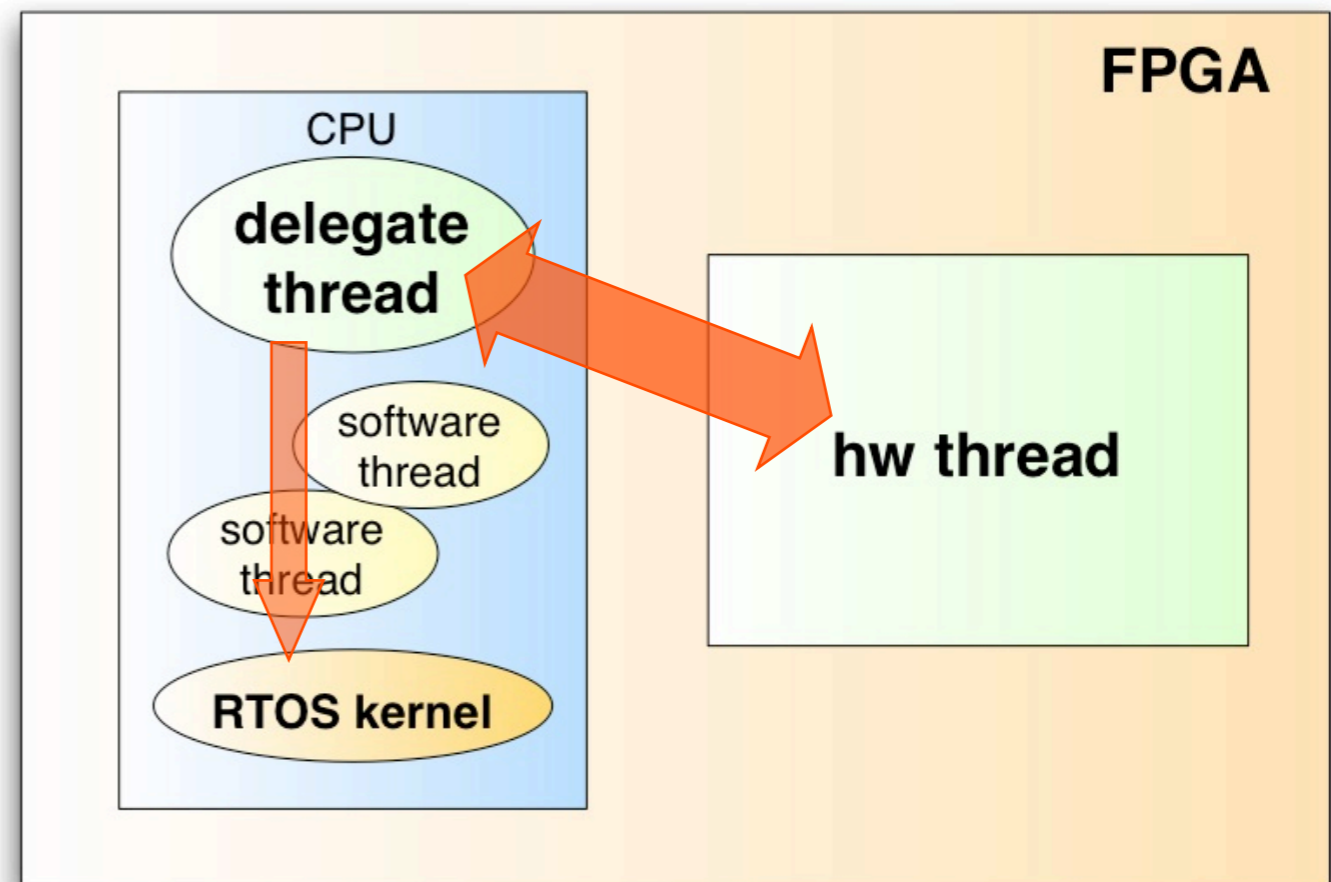
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- no modification of the kernel required
- extremely flexible
- transparent to kernel and other threads



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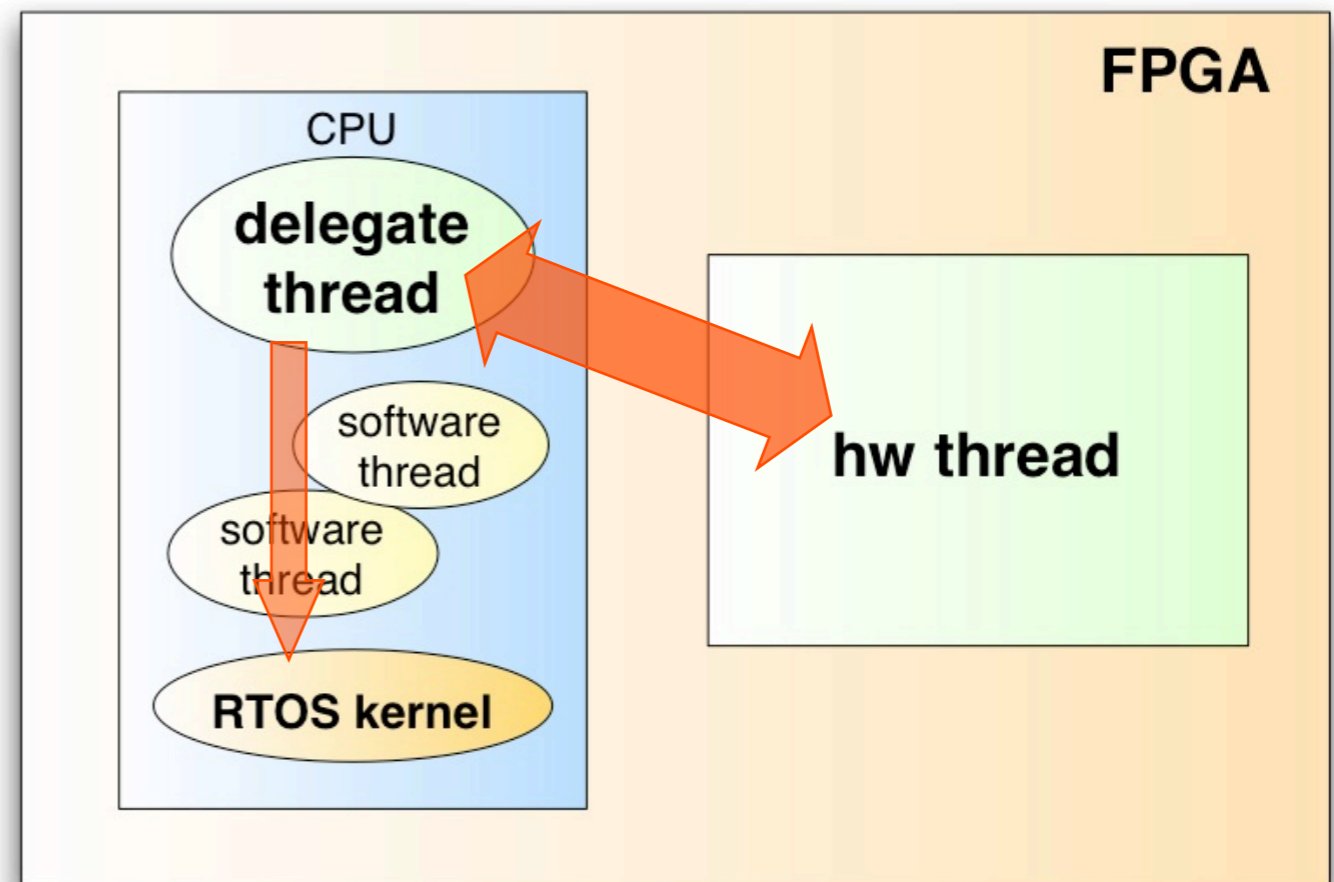
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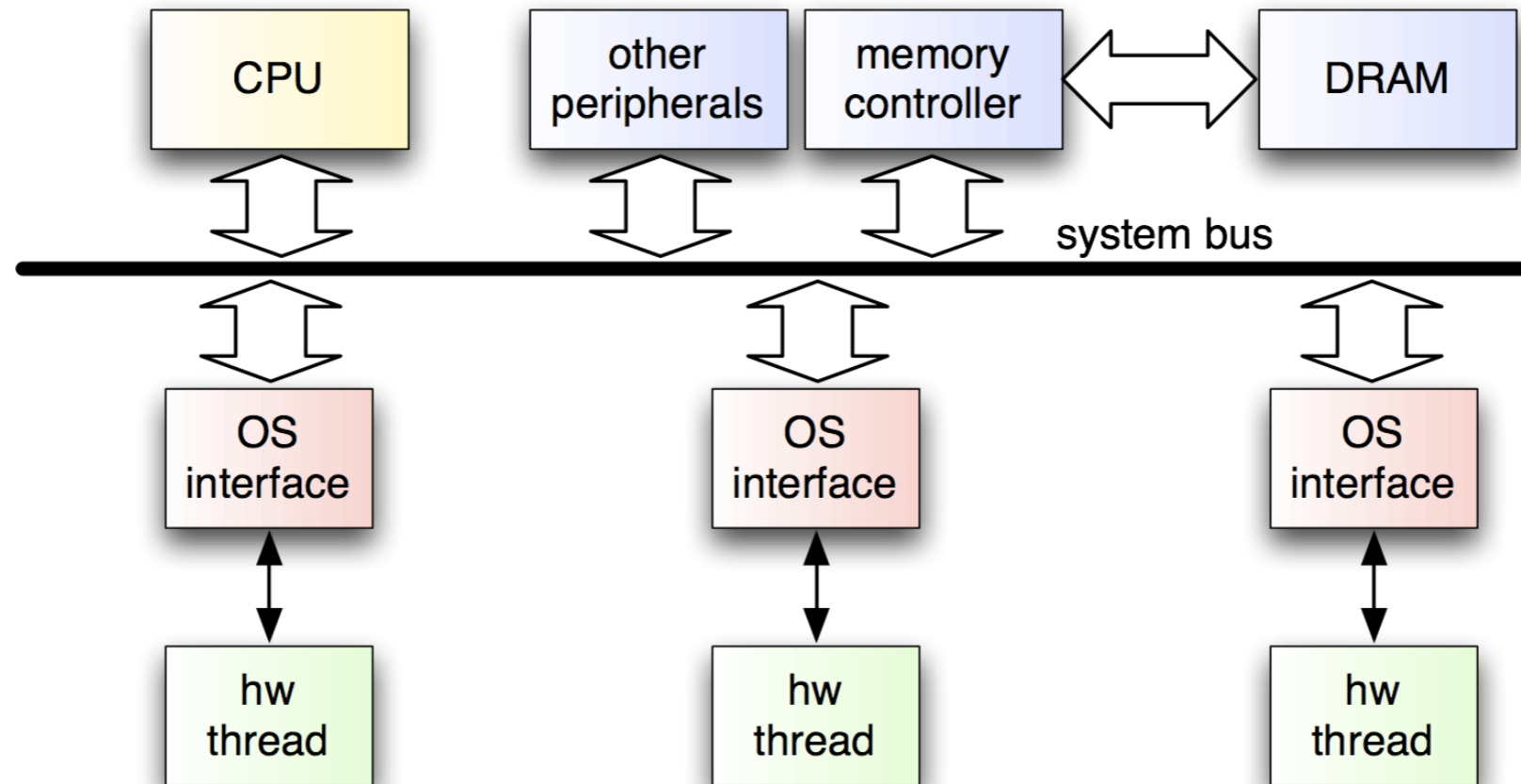
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■ drawbacks

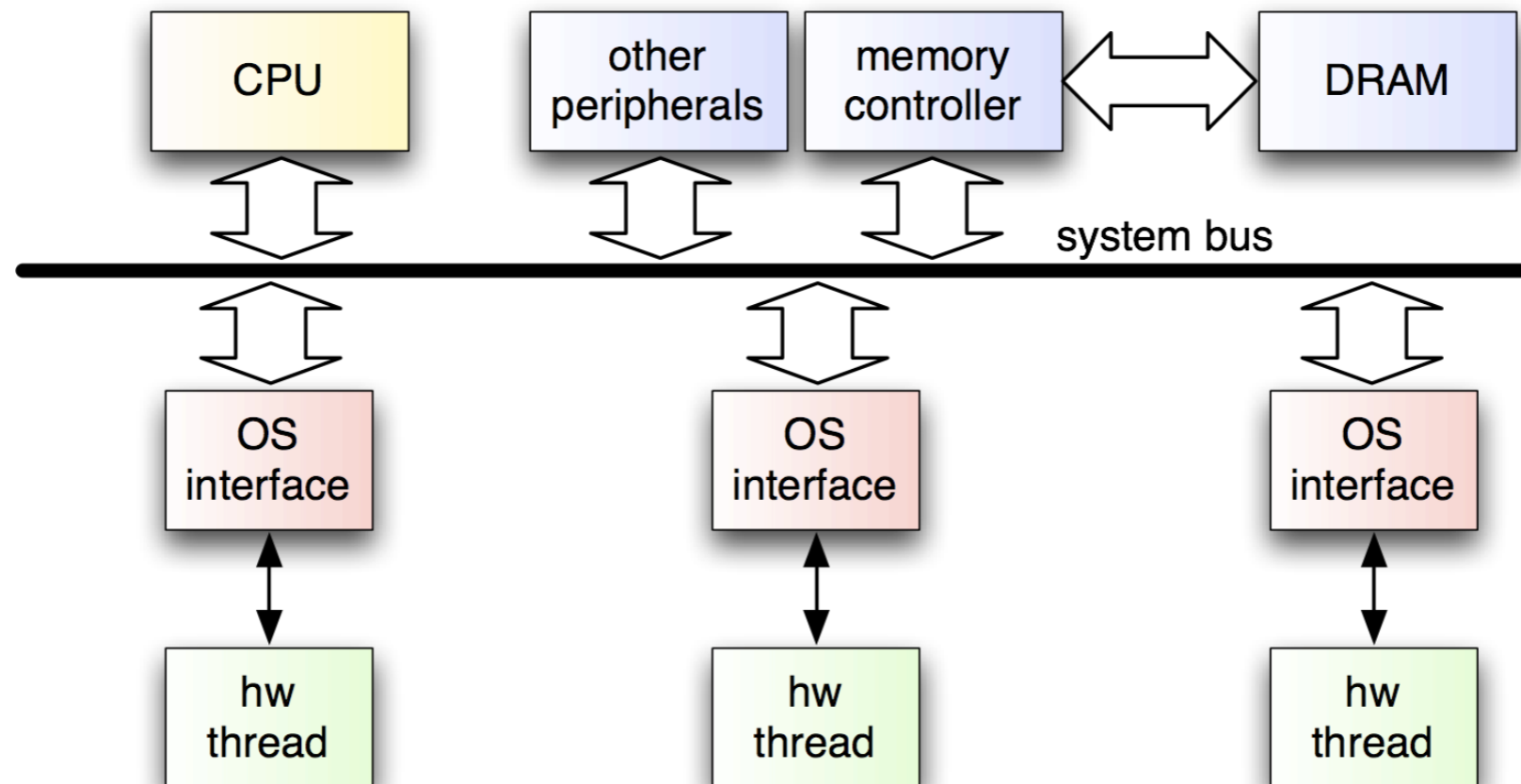
- increased overhead due to interrupt processing and context switch



Hardware Support for Message Passing

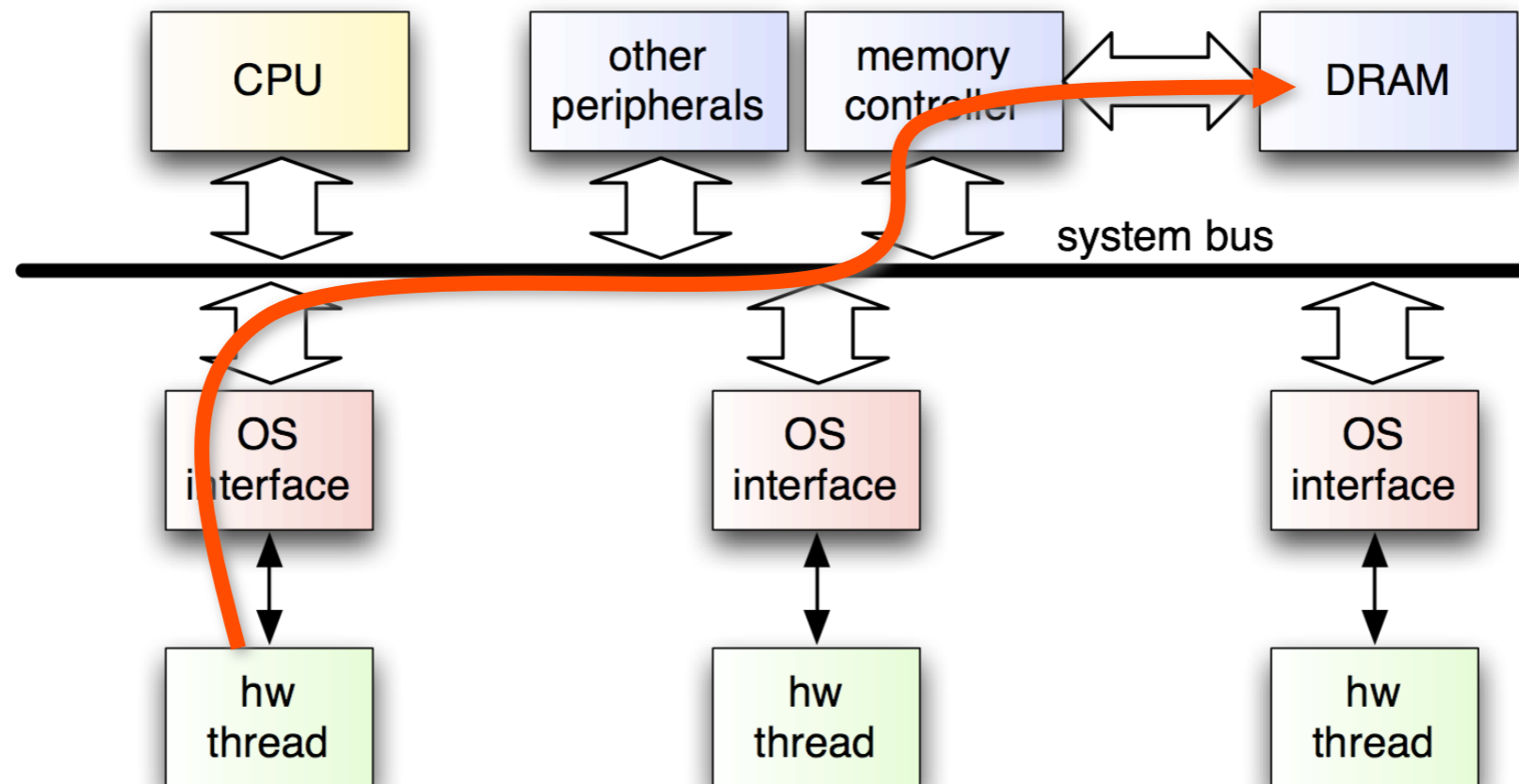


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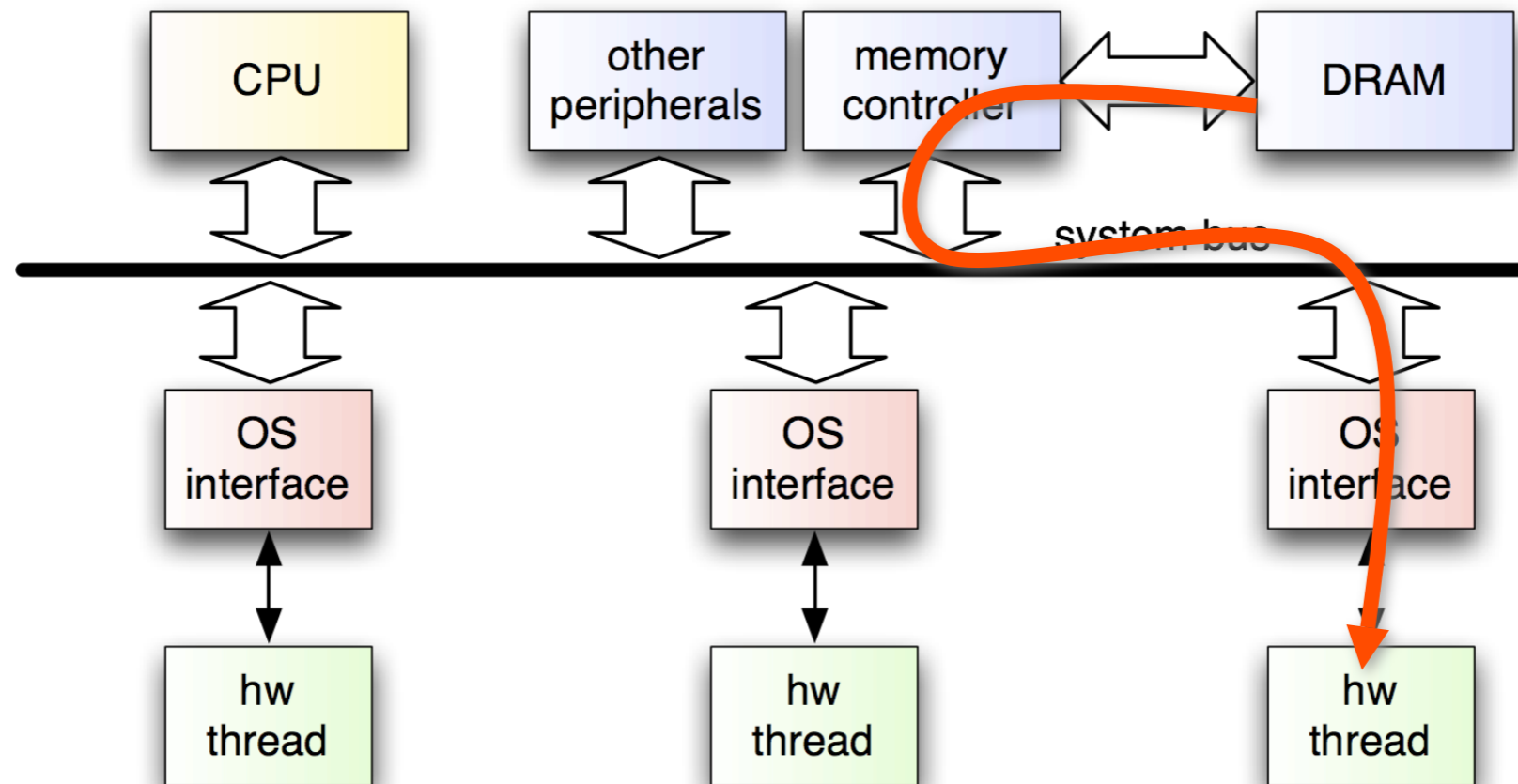
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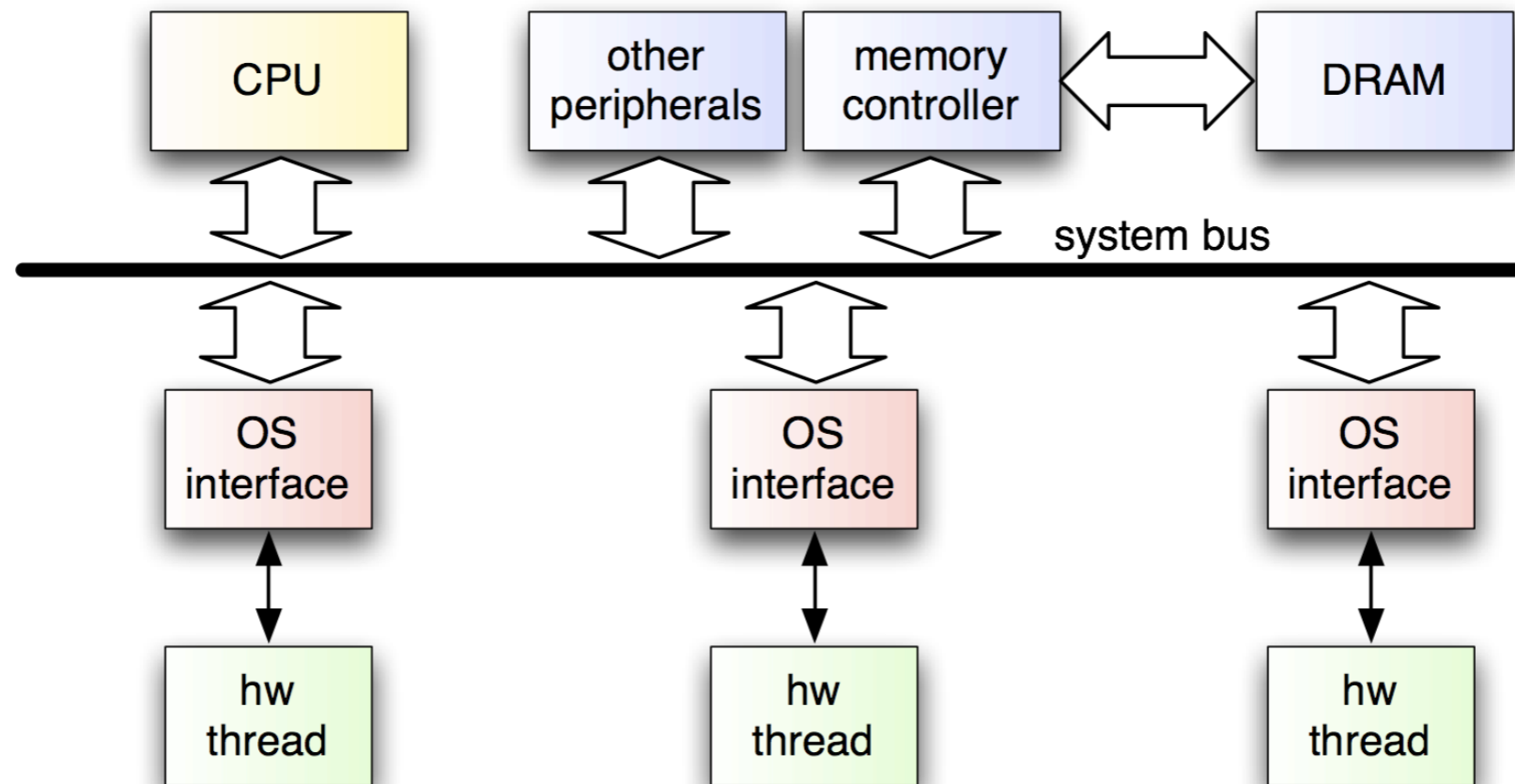
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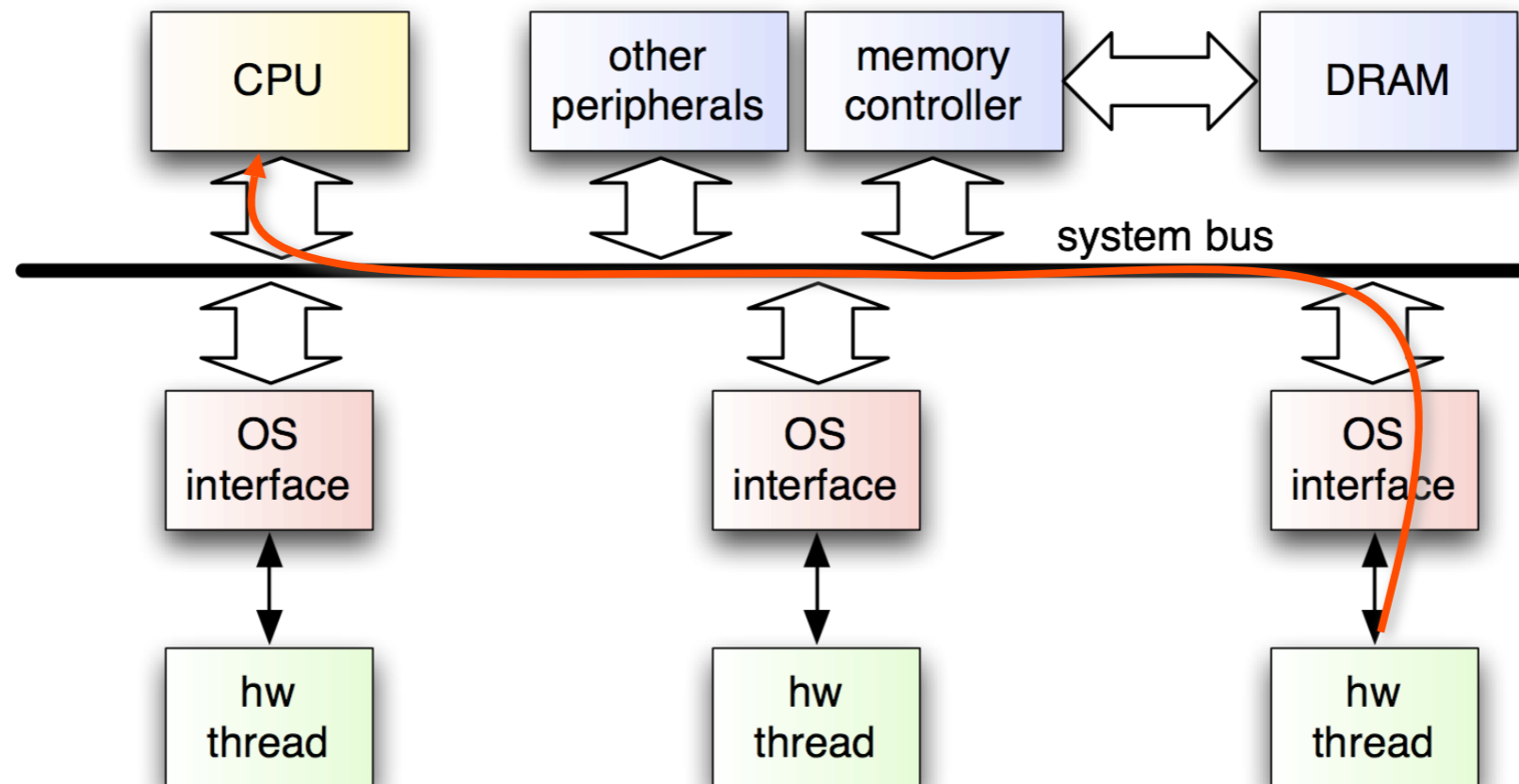
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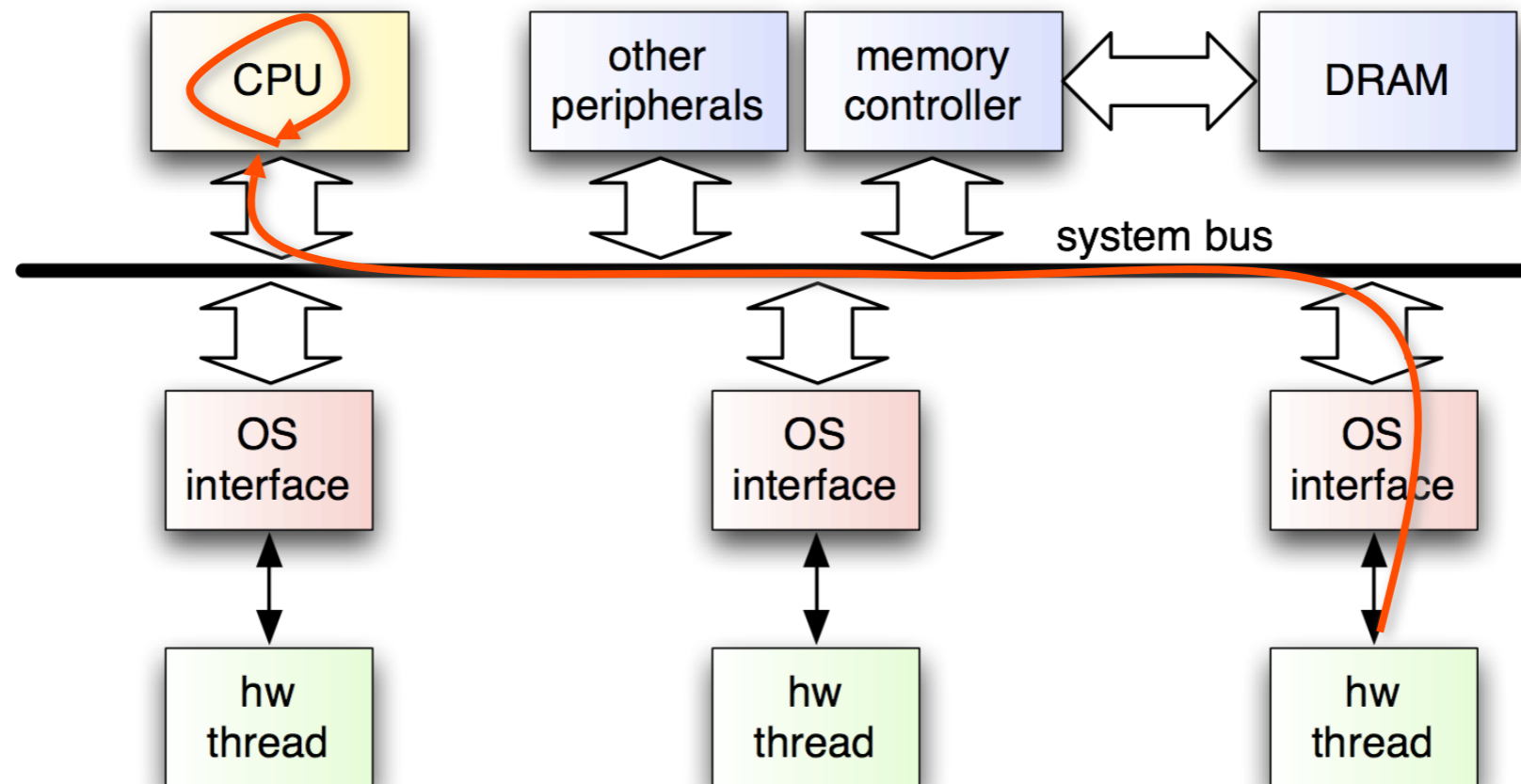
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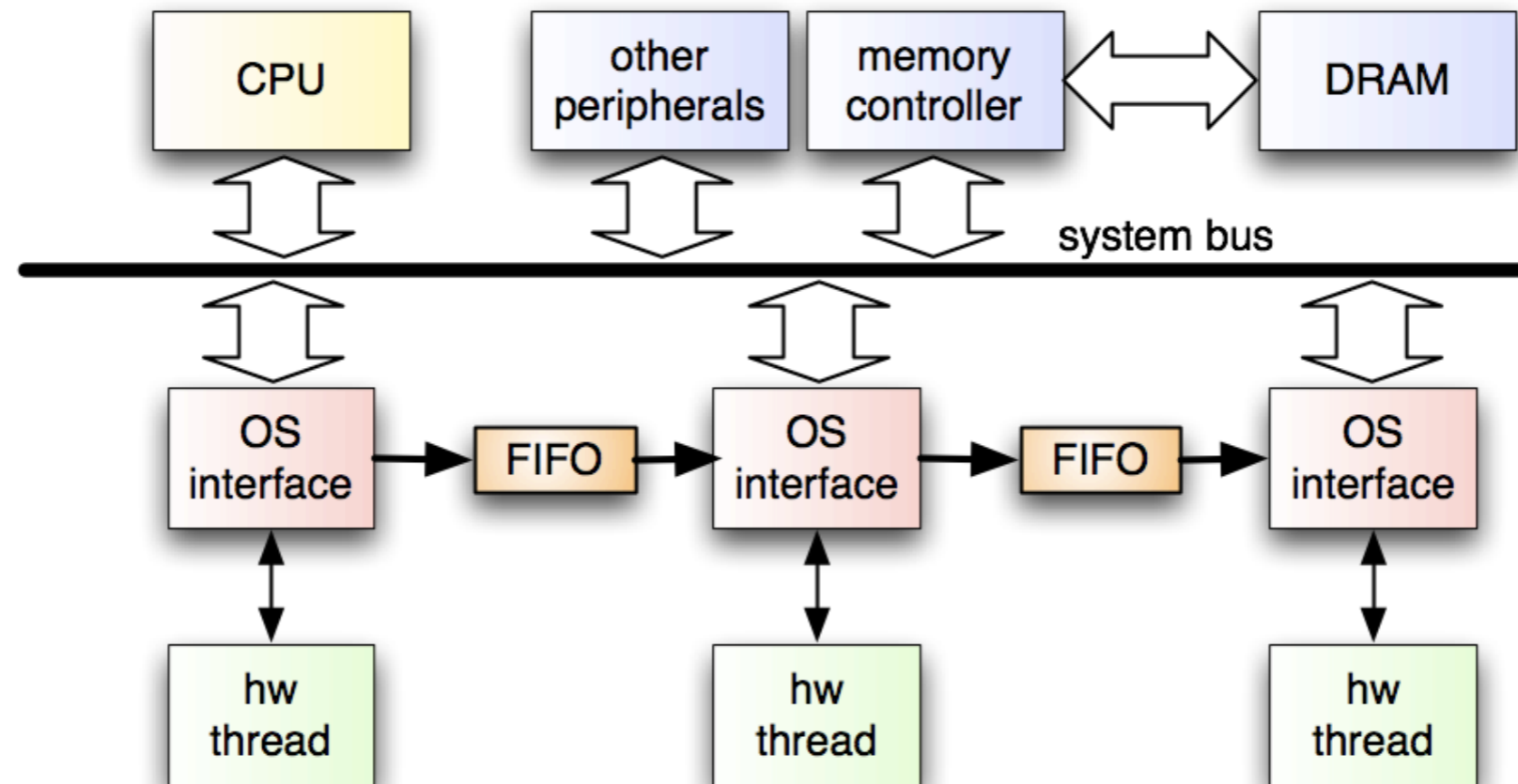
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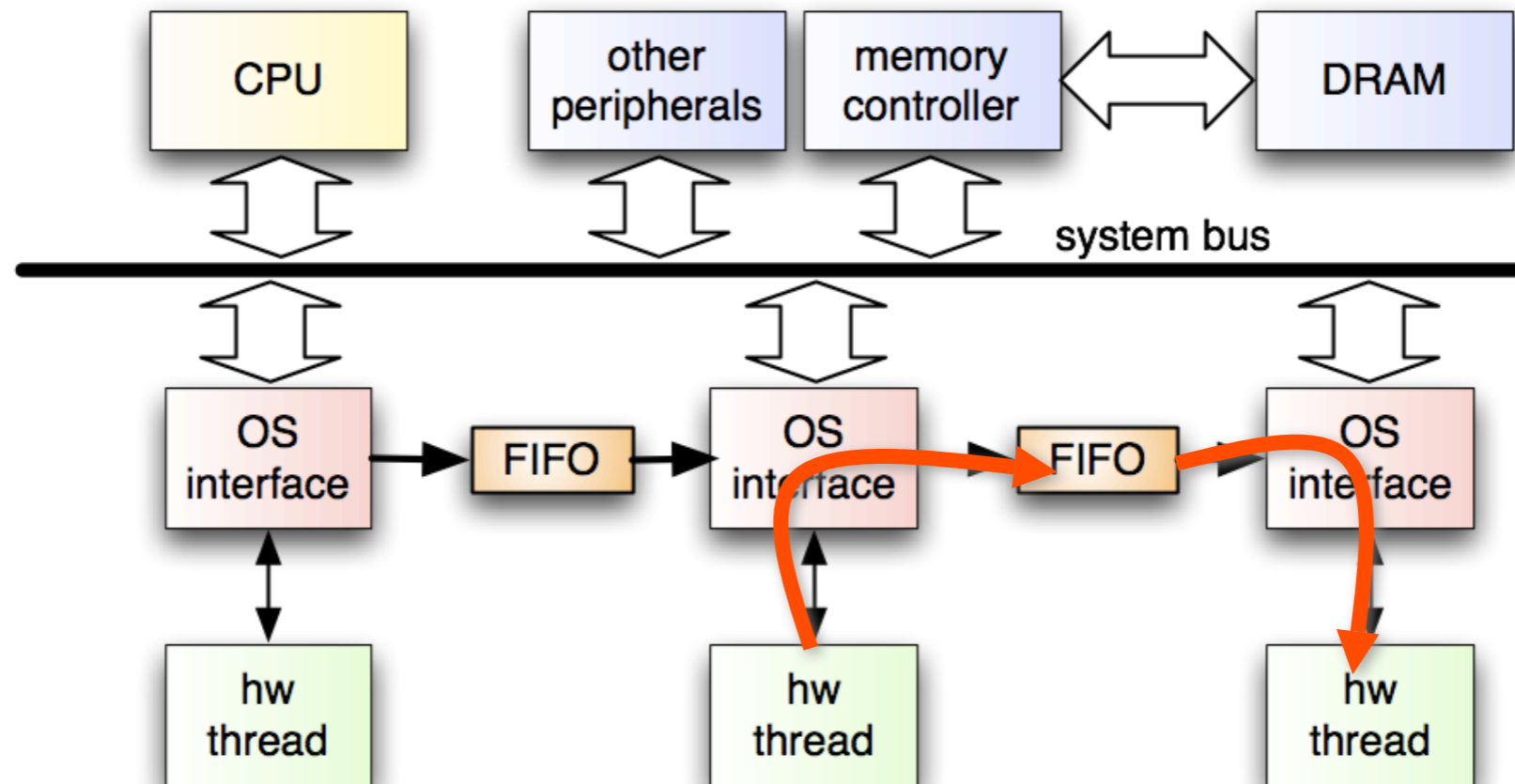
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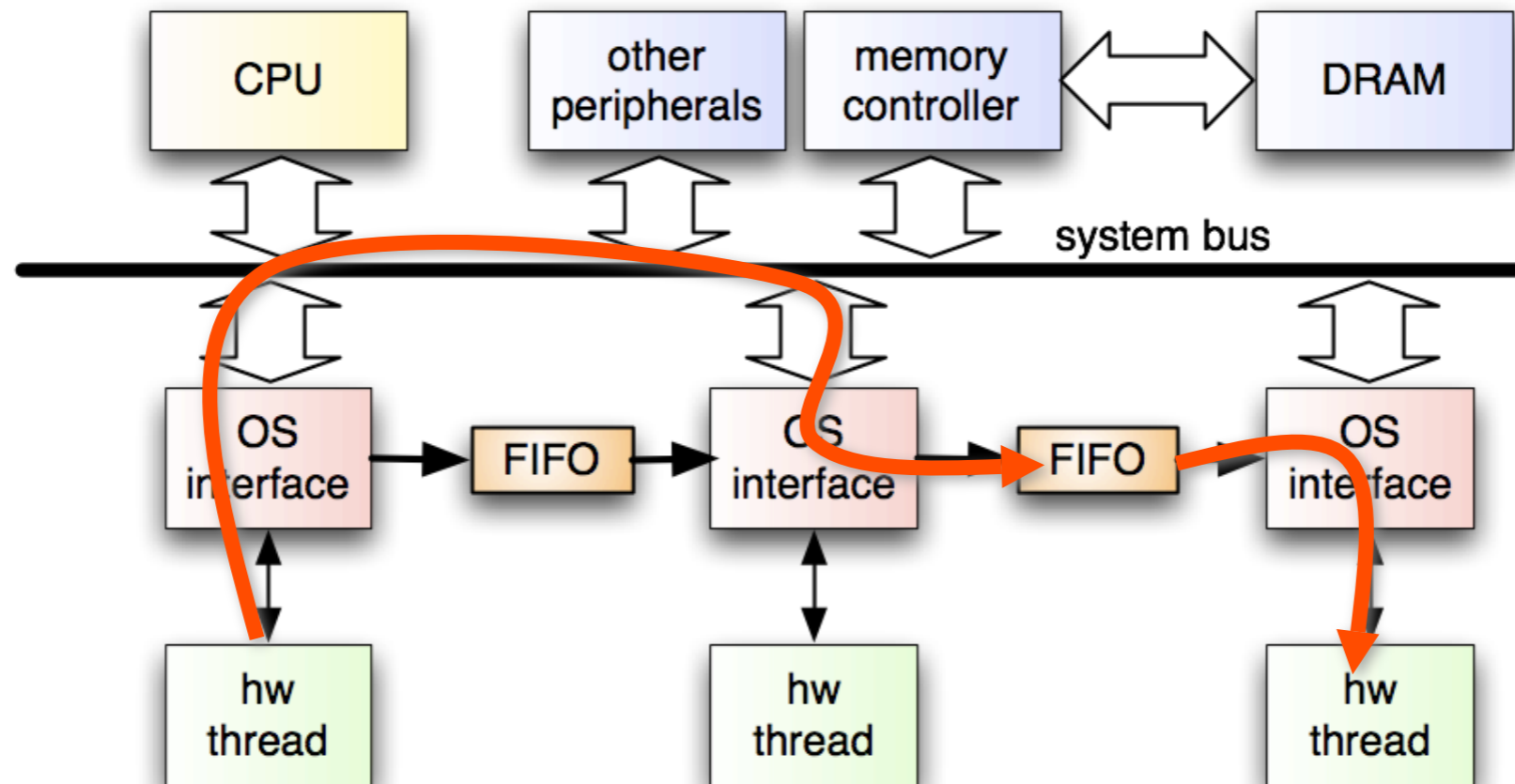
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- transparently supported by existing message queue API
- message routing dependent on current thread location (planned)

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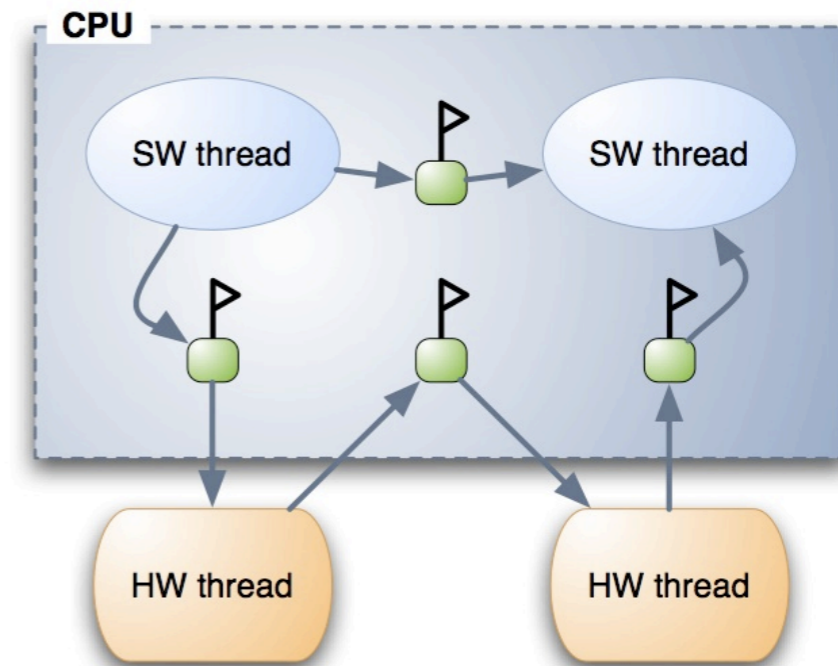


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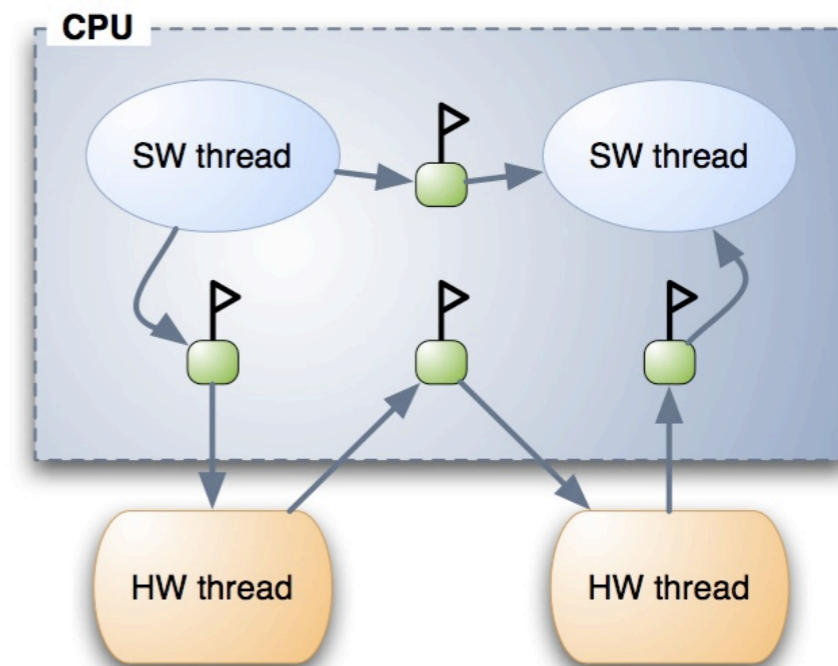
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Synchronization Overheads



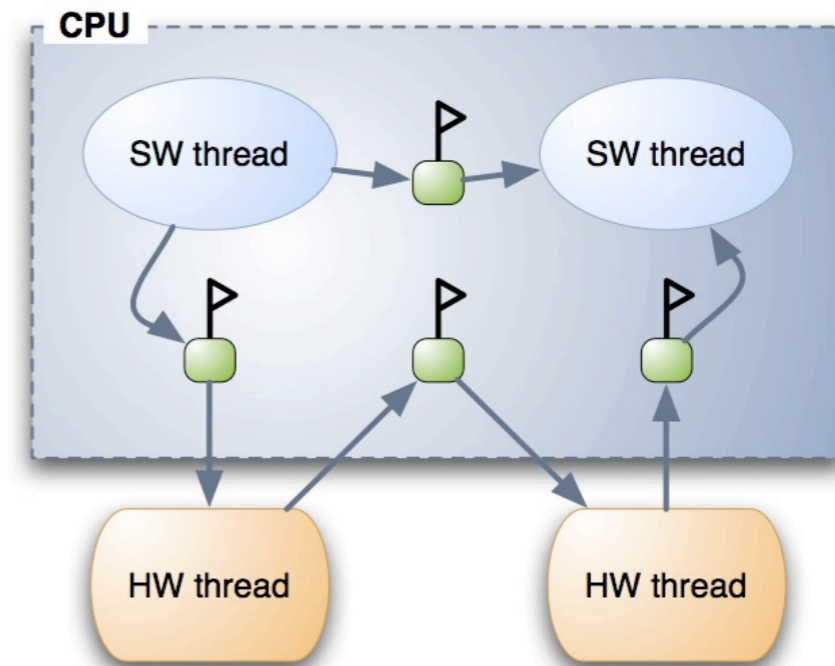
Synchronization Overheads

- synthetic hardware and software threads
 - semaphore and mutex processing time (post → wait / unlock → lock)



Synchronization Overheads

- synthetic hardware and software threads
 - semaphore and mutex processing time (post → wait / unlock → lock)
- OS calls involving hardware exhibit higher latencies
- limited impact on system performance
 - logic resources mainly used for heavy data-parallel processing
 - less synchronization-intensive control dominated code



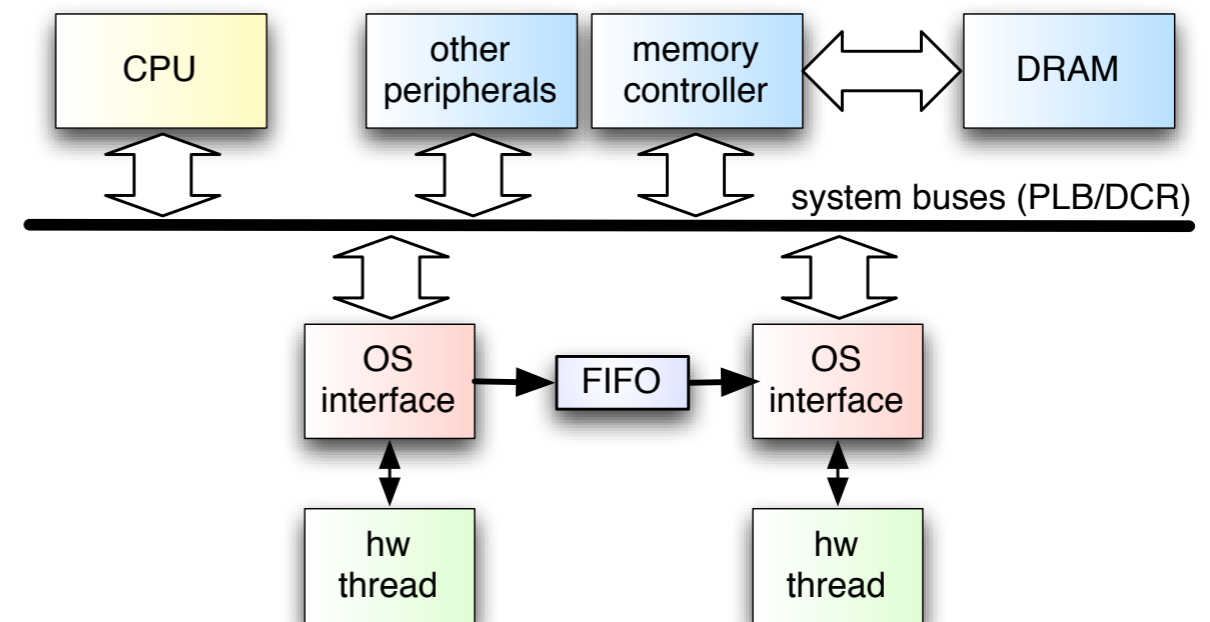
Configuration	with data cache		without data cache	
	semaphore	mutex	semaphore	mutex
SW → SW	3.39	4.53	29.05	43.99
SW → HW	4.71	6.29	30.49	47.43
HW → SW	10.74	14.49	82.90	100.23
HW → HW	11.90	14.60	83.13	101.49

All values are given in μs

Communication Performance

Operation	with data cache		without data cache	
	μs	MB/s	μs	MB/s
MEM→HW (burst read)	45.74	170.80	46.41	168.34
HW→MEM (burst write)	40.54	192.71	40.55	192.66
MEM→SW→MEM (memcpy)	132.51	58.96	625.00	12.50
hardware FIFOs → HW→HW (mbox read)	61.42	127.20	61.42	127.20
HW→HW (mbox write)	61.45	127.14	61.45	127.14
software mailboxes → SW→HW (mbox read)	58500	0.13	374000	0.02
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All operations were run for 8 kBytes of data

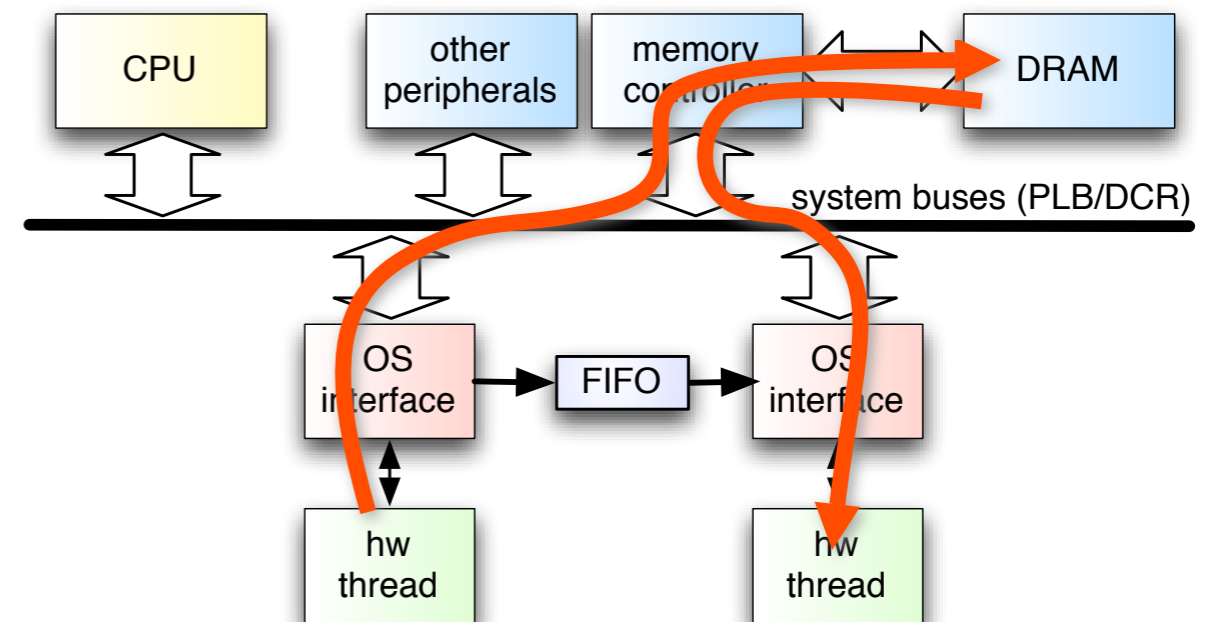


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software
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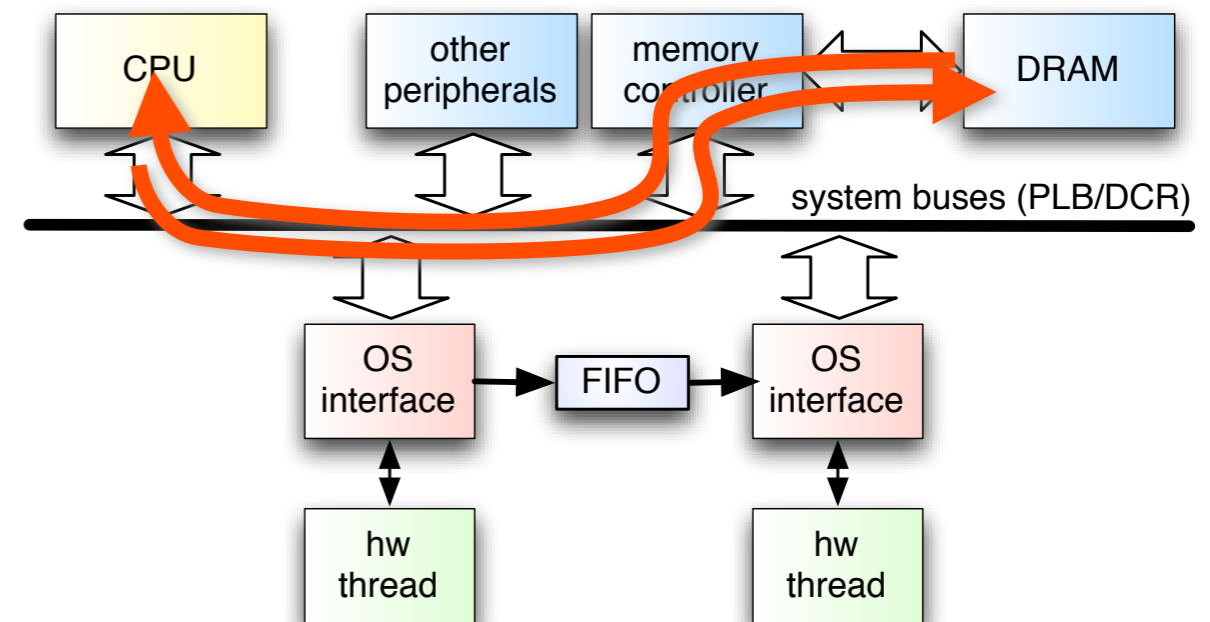


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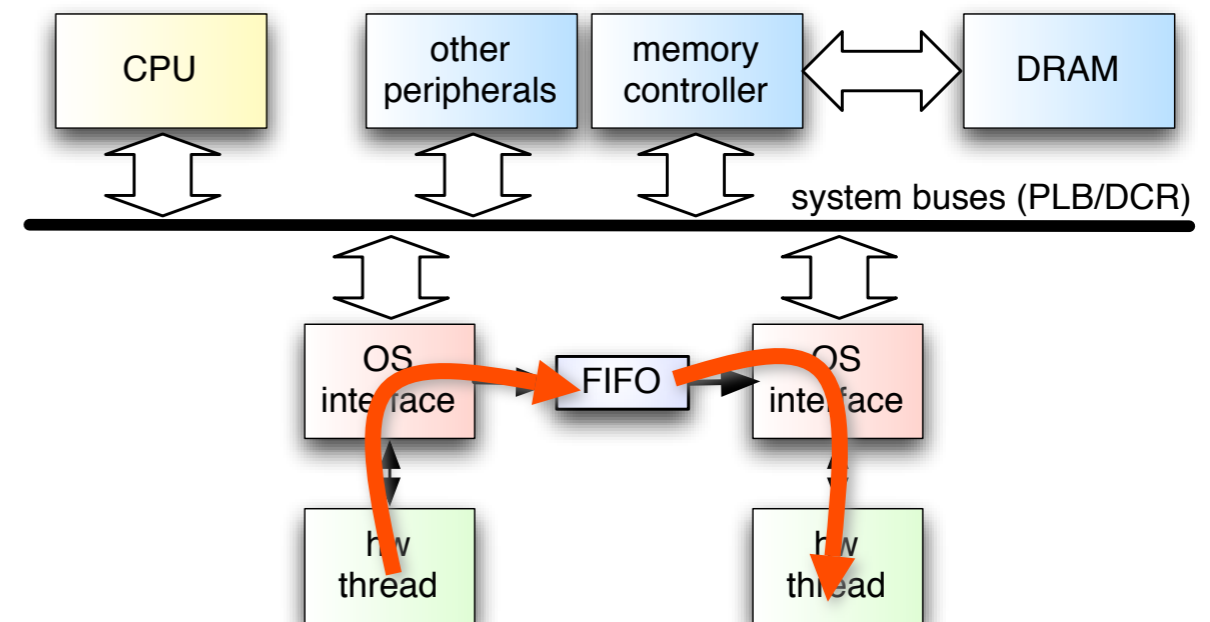
hardware
FIFOs
software
mailboxes



Communication Performance

Operation	with data cache		without data cache	
	μs	MB/s	μs	MB/s
MEM→HW (burst read)	45.74	170.80	46.41	168.34
HW→MEM (burst write)	40.54	192.71	40.55	192.66
MEM→SW→MEM (memcpy)	132.51	58.96	625.00	12.50
hardware FIFOs → HW→HW (mbox read)	61.42	127.20	61.42	127.20
hardware FIFOs → HW→HW (mbox write)	61.45	127.14	61.45	127.14
software mailboxes → SW→HW (mbox read)	58500	0.13	374000	0.02
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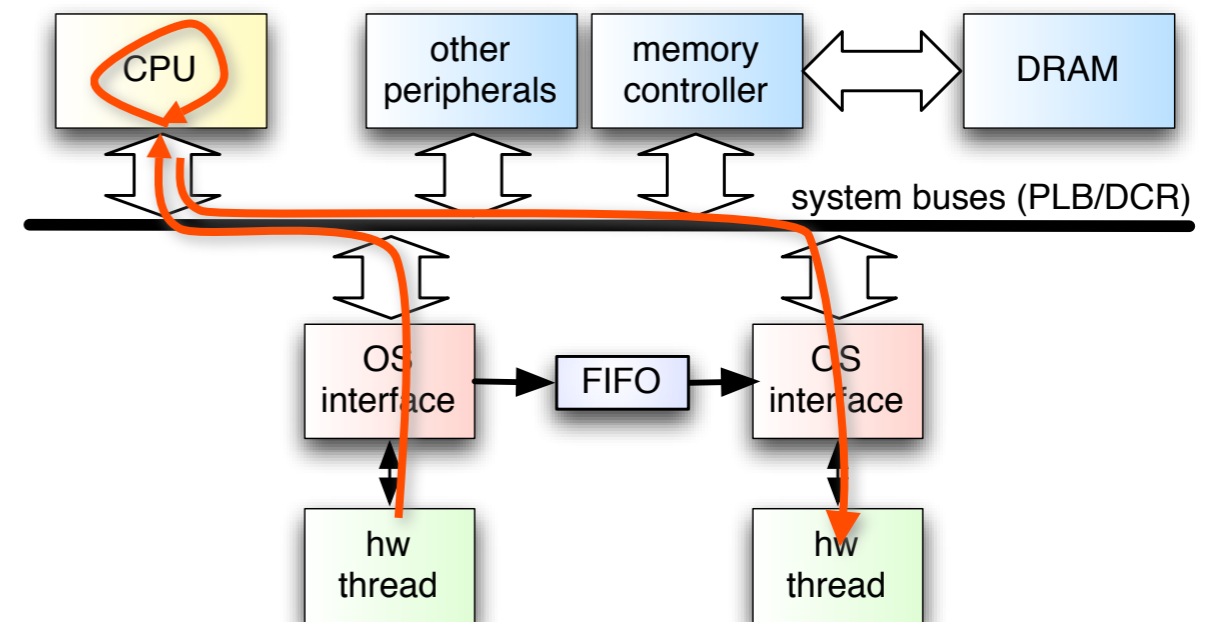
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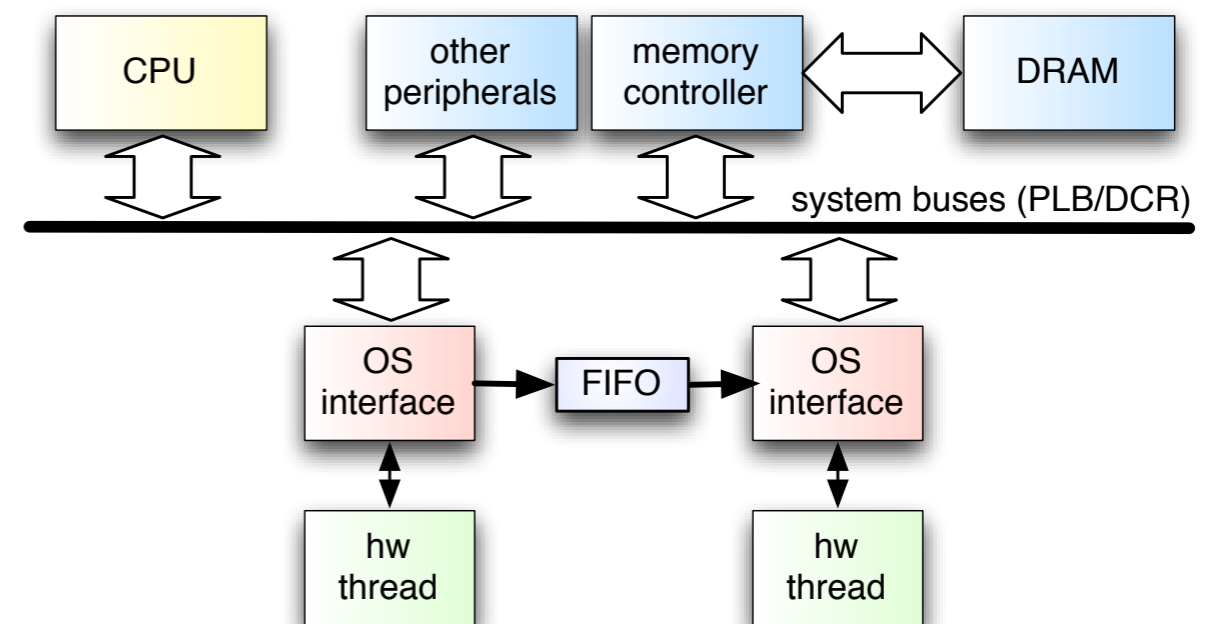
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All operations were run for 8 kBytes of data

■ comparison between memory access and FIFO transfers

- FIFOs are faster for HW thread to HW thread communications (+40%)
- no additional load on memory system or CPU
- improves thread-parallelism



Conclusion & Outlook

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- common set of high-level communication and synchronization objects for hard- and software unifies programming model
- existing operating systems can be extended with mechanisms for low-level communication and synchronization between hardware threads and kernel
- acceptable performance in benchmarks and larger case studies

Conclusion & Outlook

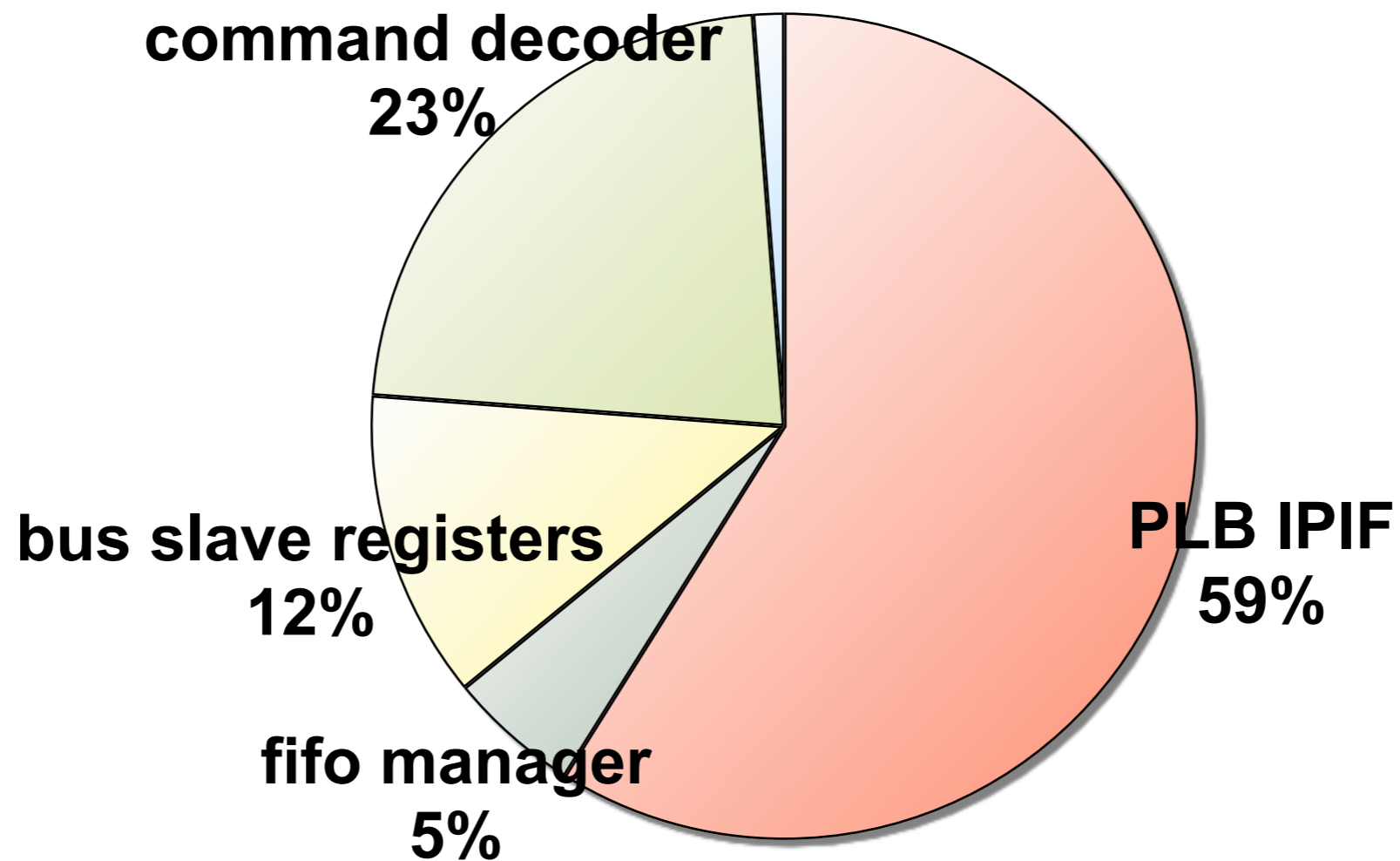
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- existing operating systems can be extended with mechanisms for low-level communication and synchronization between hardware threads and kernel
- acceptable performance in benchmarks and larger case studies

- future work
 - extension of hardware FIFOs to allow direct access from software threads
 - fusion of shared memory and message-passing interfaces to hardware threads

Thank you

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OS Overheads (Area)



- total OSIF slice count: 1213 slices
 - most of this taken up by PLB IPIF logic

Supported OS Calls

■ Semaphores (counting and binary)

- reconos_semaphore_post()
- reconos_semaphore_wait()

basic synchronization
primitives

■ Mutexes

- reconos_mutex_lock()
- reconos_mutex_trylock()
- reconos_mutex_unlock()
- reconos_mutex_release()

synchronize access to
mutual exclusive operations
(critical sections)

■ Condition Variables

- reconos_cond_wait()
- reconos_cond_signal()
- reconos_cond_broadcast()

allow waiting until arbitrary
conditions are satisfied

■ Mailboxes

- reconos_mbox_get()
- reconos_mbox_tryget()
- reconos_mbox_put()
- reconos_mbox_tryput()

message passing primitives
(blocking and not blocking)

■ Memory access

- reconos_read()
- reconos_write()
- reconos_read_burst()
- reconos_write_burst()

CPU-independent access
to the entire system address
space (memory and peripherals)

handled in
software
(via delegate
thread)

handled in
hardware
(via system
bus / point-
to-point
links)

ReconOS Software API (POSIX)

- standard POSIX thread creation
- ReconOS hardware thread creation

```
mqd_t my_mbox;  
sem_t my_sem;
```

```
pthread_t      thread;  
pthread_attr_t thread_attr;
```

...

```
pthread_attr_init(&thread_attr);
```

```
pthread_create(  
    &thread,           // thread object  
    &thread_attr,     // attributes  
    thread_entry,     // entry point  
    ( void * ) data  // entry data  
);
```

```
mqd_t my_mbox;  
sem_t my_sem;  
reconos_res_t thread_resources[2] = {  
    { &my_mbox, POSIX_MQD_T },  
    { &my_sem,  POSIX_SEM_T  }  
};
```

```
rthread      thread;  
pthread_attr_t thread_swattr;  
rthread_attr_t thread_hwattr;
```

...

```
pthread_attr_init(&thread_swattr);  
rthread_attr_init(&thread_hwattr);  
rthread_attr_setslotnum(&thread_hwattr, 0);  
rthread_attr_setresources(&thread_hwattr,  
                           thread_resources, 2);
```

```
rthread_create(  
    &thread,           // thread object  
    &thread_swattr,   // software attributes  
    &thread_hwattr,   // hardware attributes  
    ( void * ) data  // entry data  
);
```

Multi-Cycle Commands

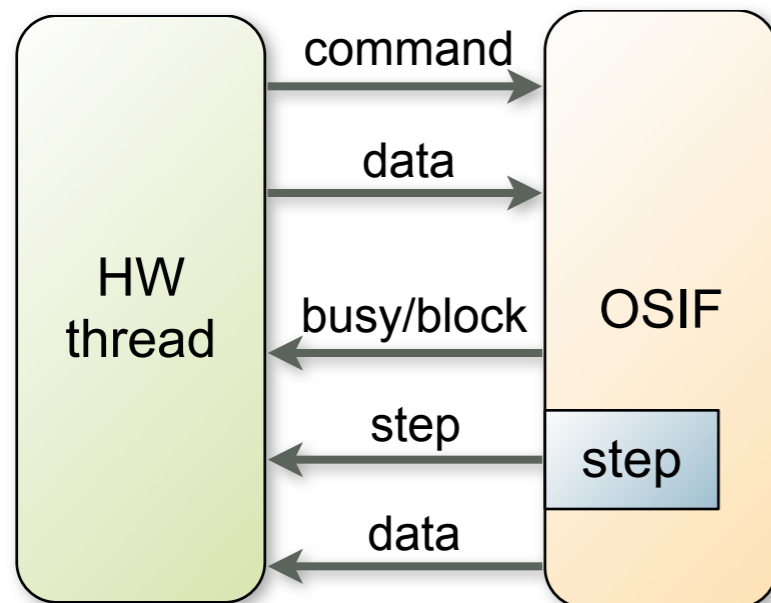
- transfer of multiple parameters and return values with a single VHDL call
- distributes execution of an FSM state across multiple clock cycles

state = A

HW thread

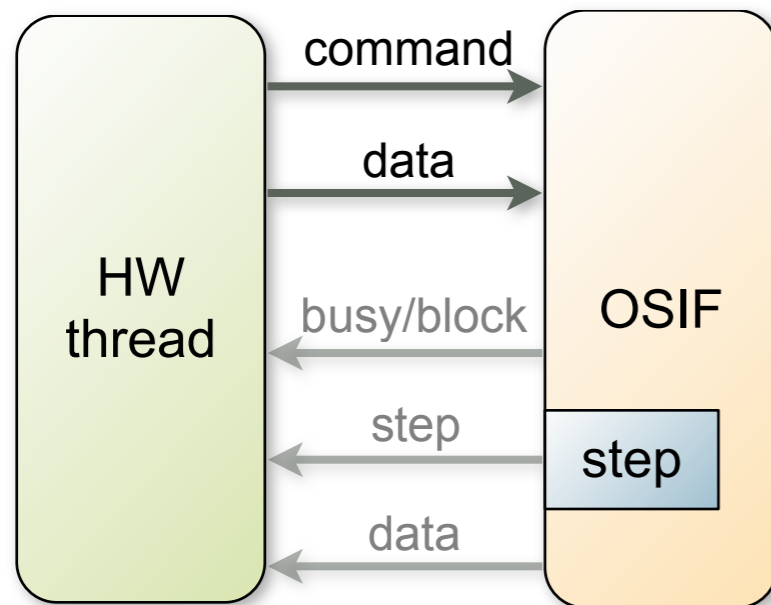
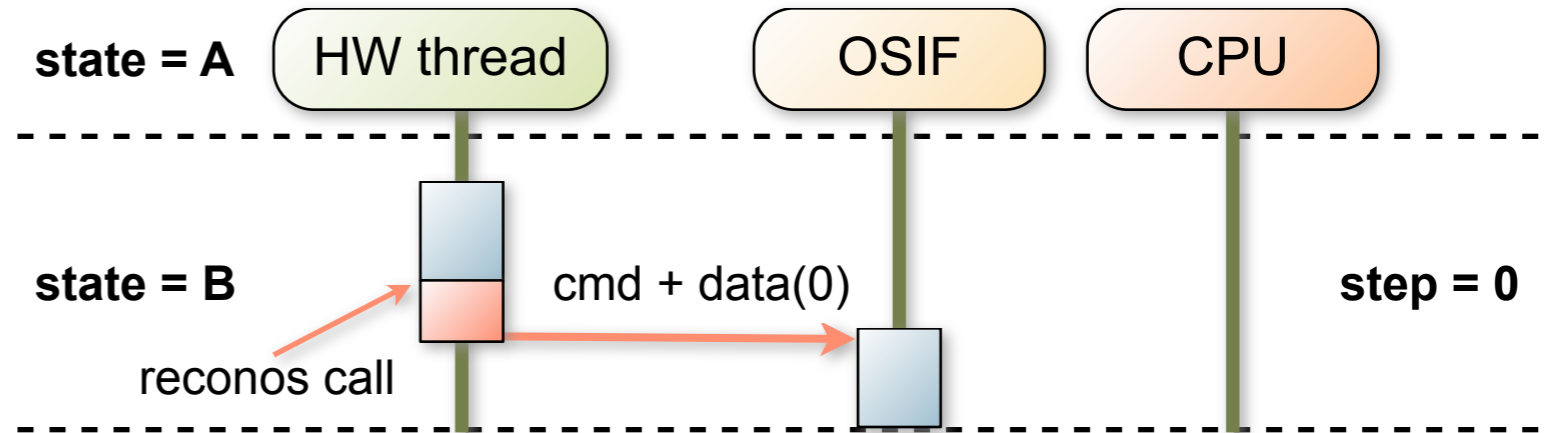
OSIF

CPU



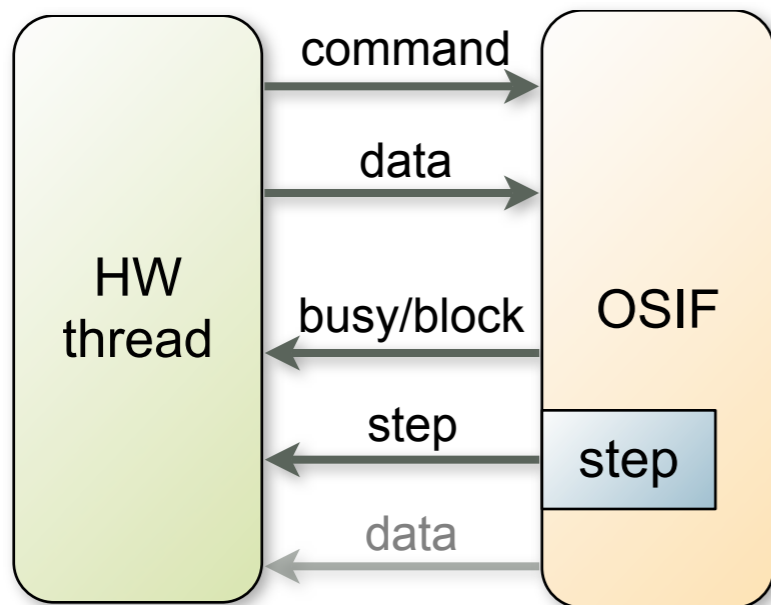
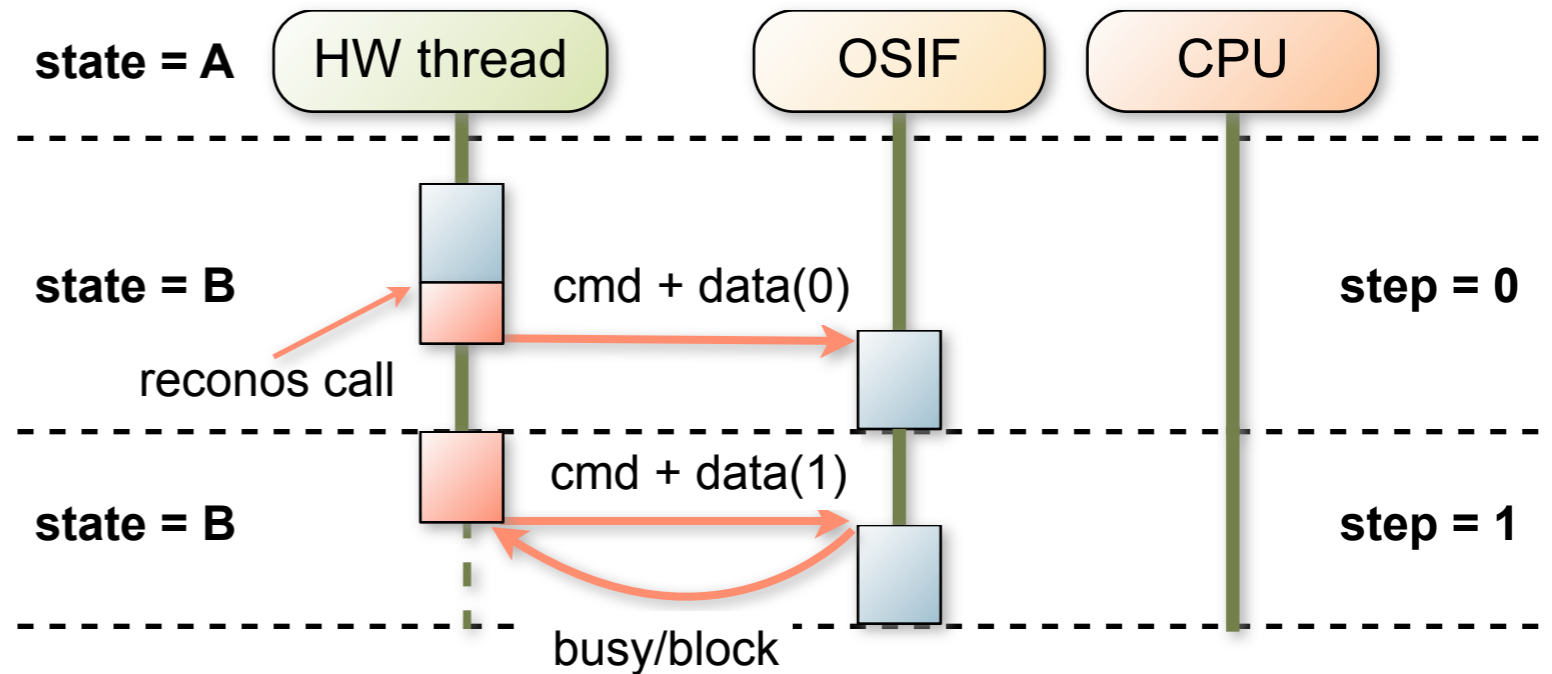
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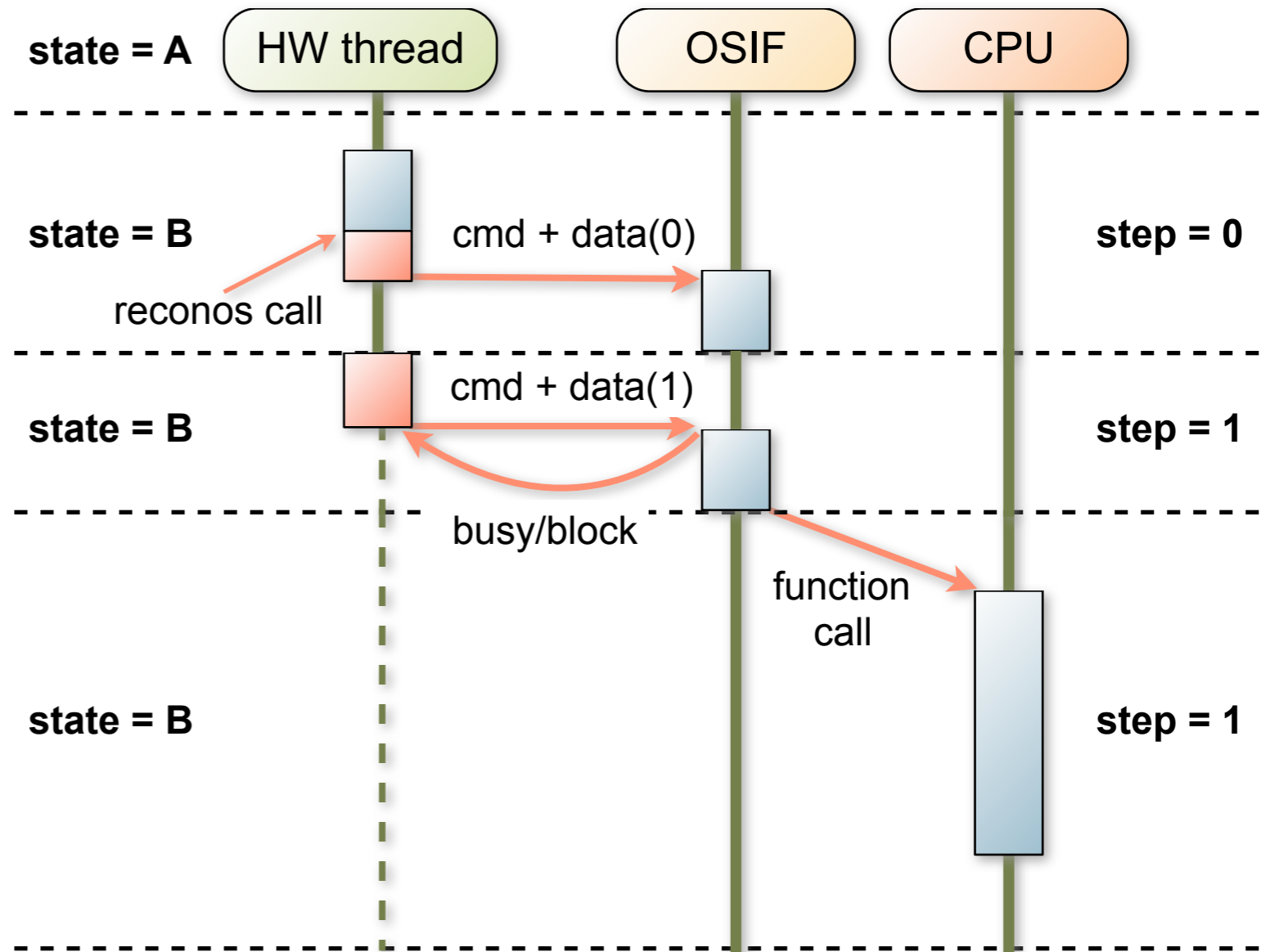
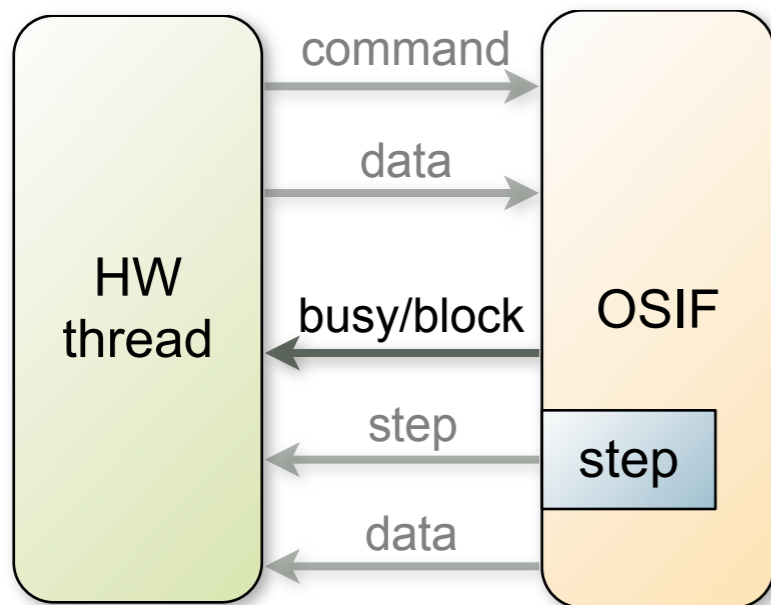
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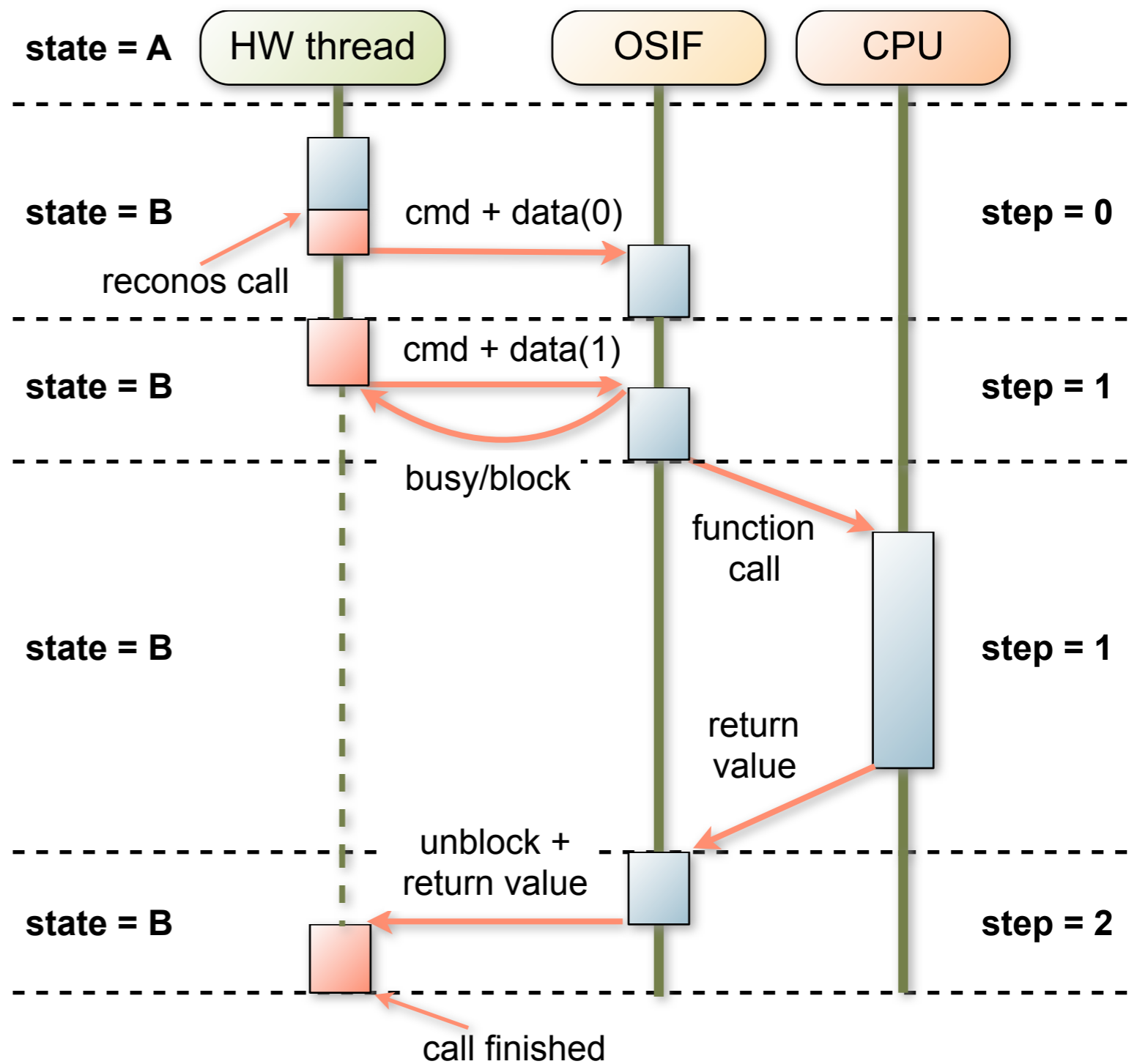
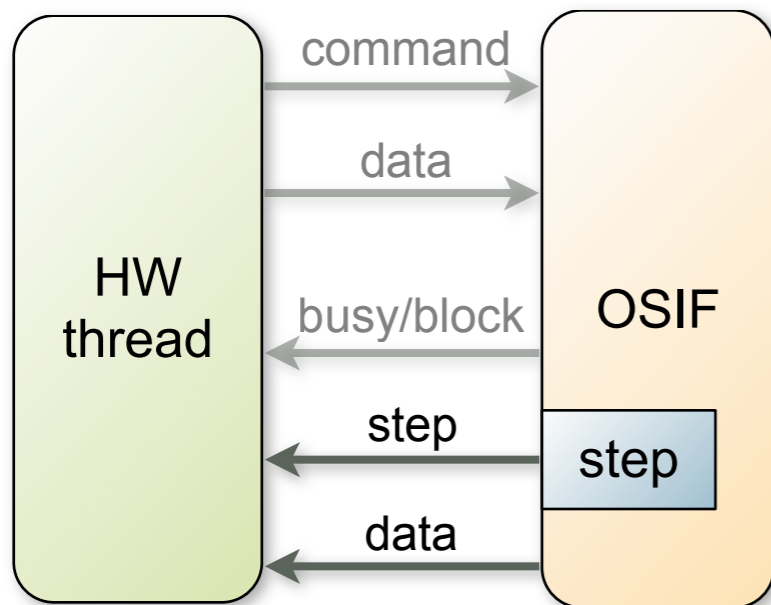
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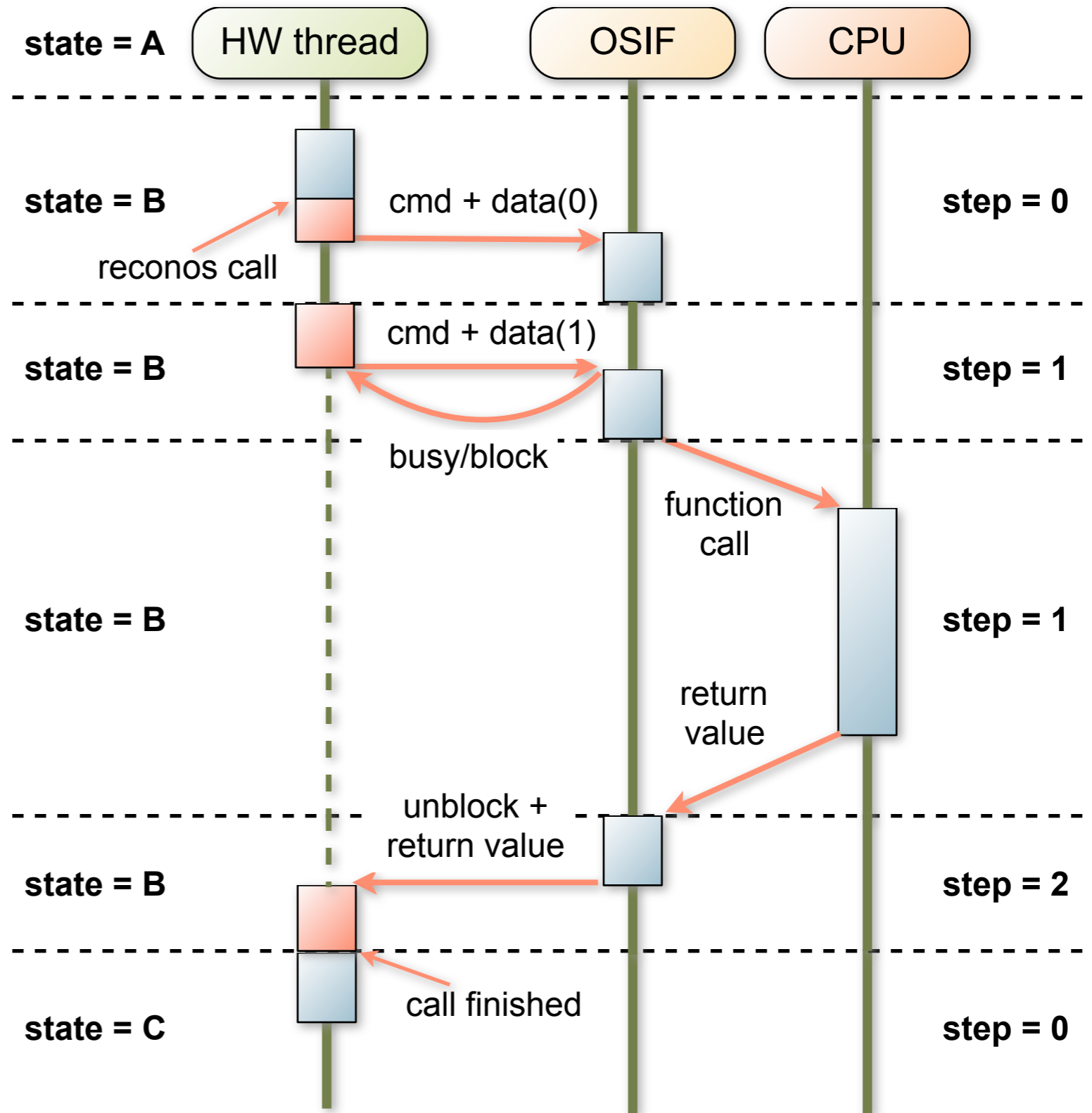
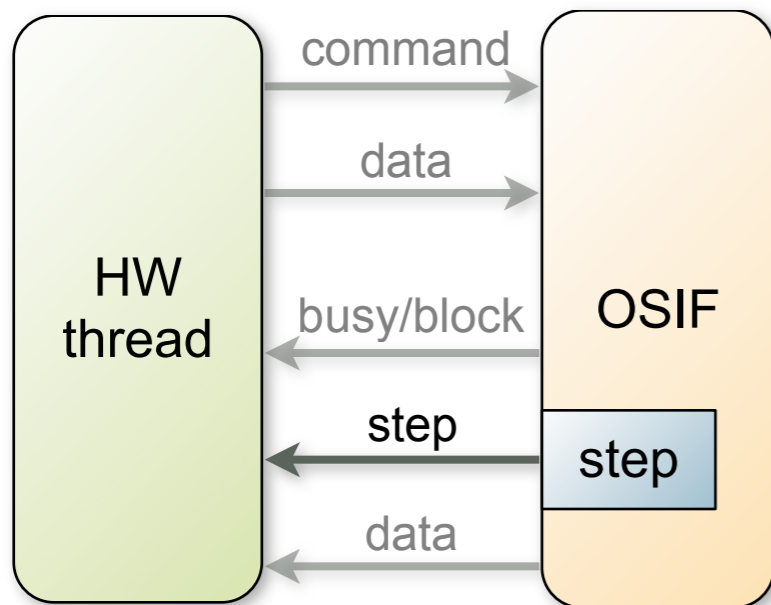
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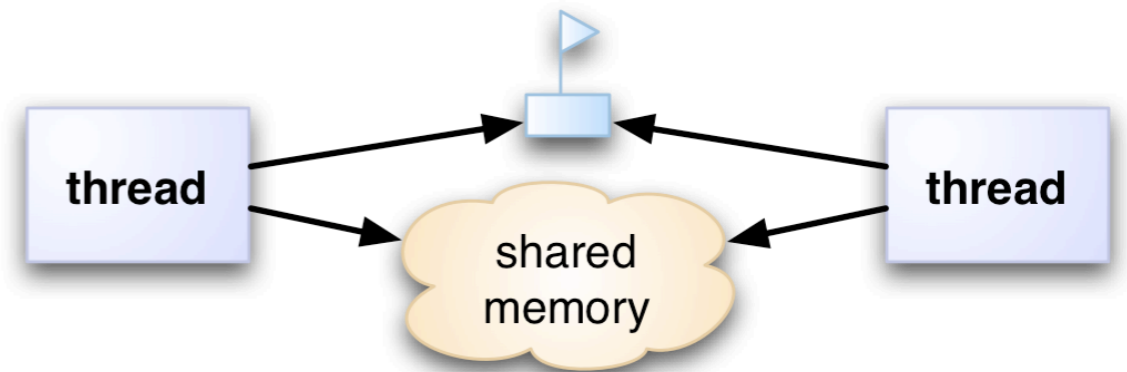


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Toolchain

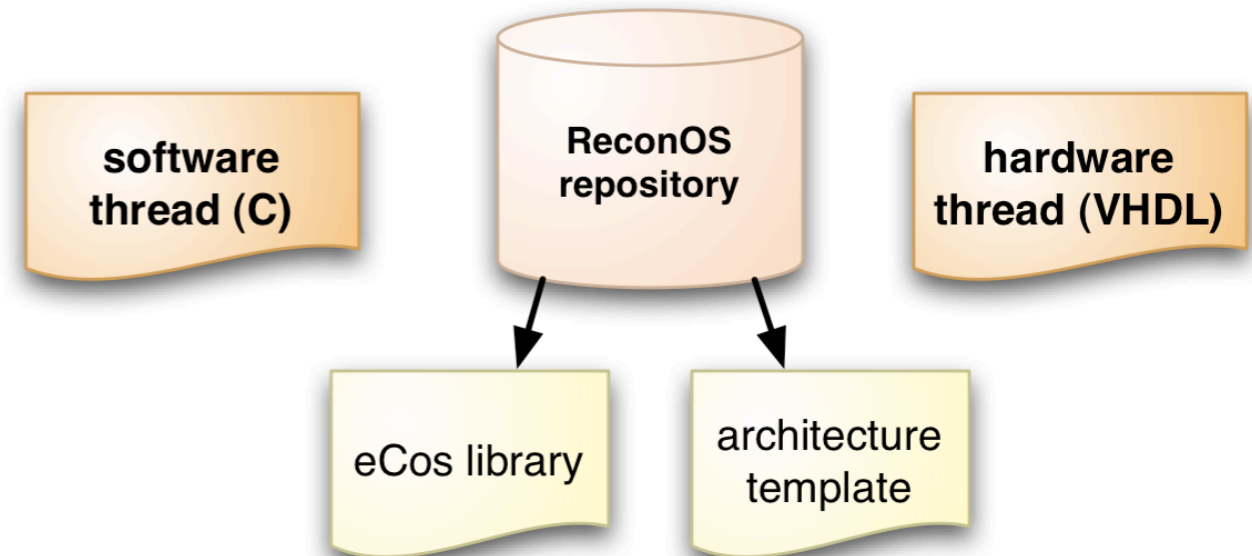


Toolchain



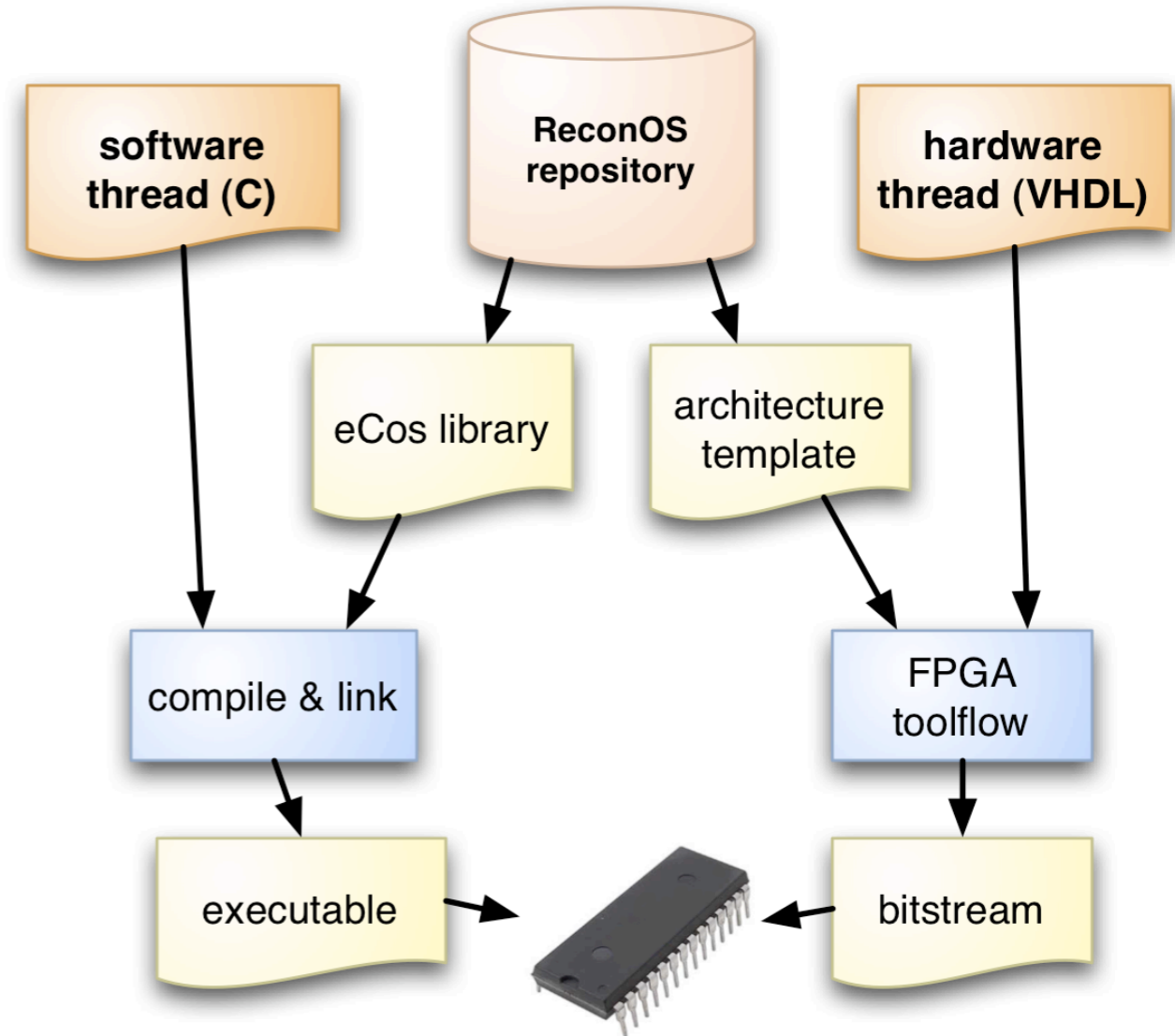
Toolchain

- software threads are written in C
 - u using the eCos software API
- hardware threads are written in VHDL
 - u using the ReconOS VHDL API
- architecture generation
 - u automatically inserts OS interfaces and hardware threads into Xilinx EDK platform templates
 - u configures and builds static eCos library



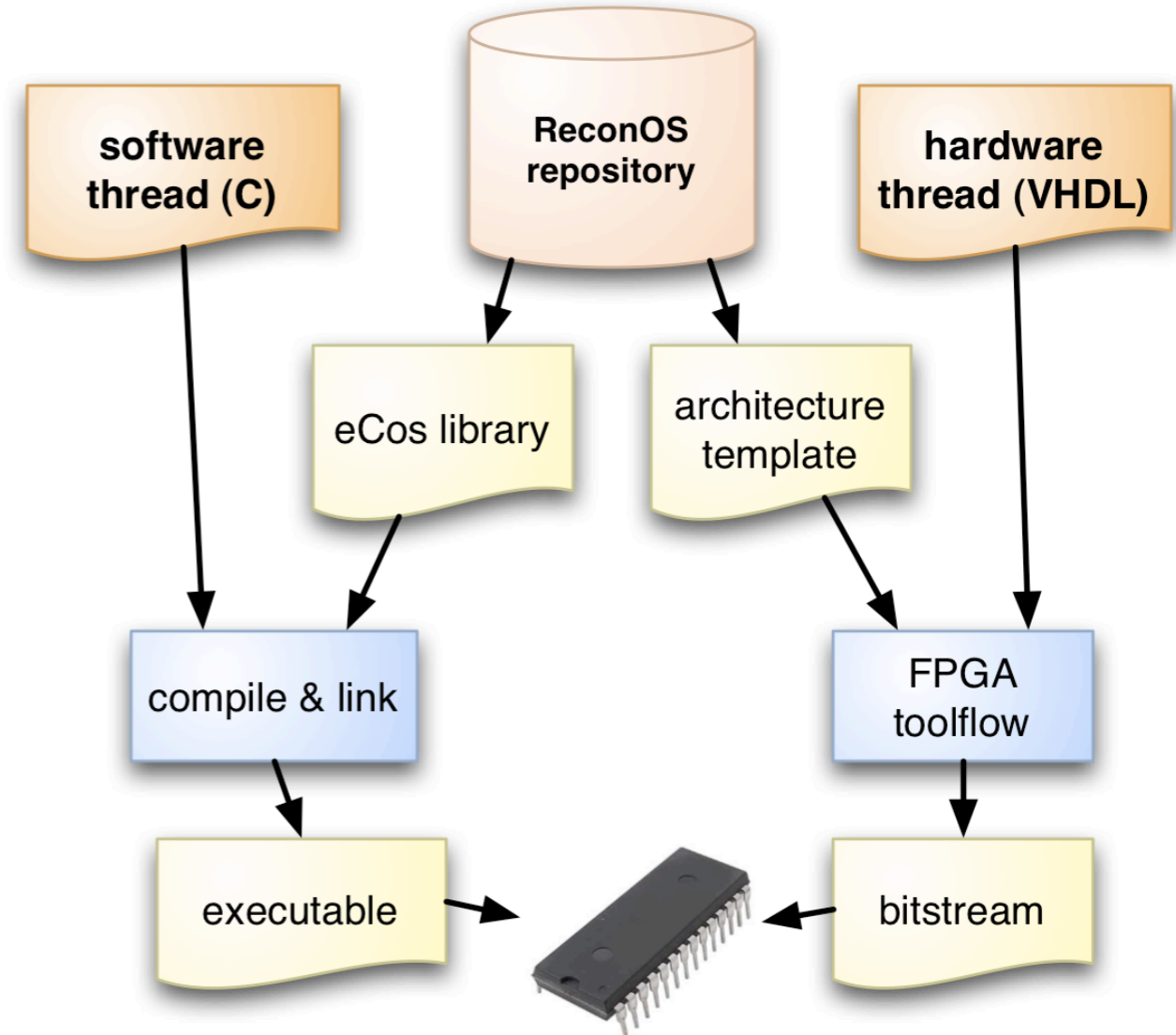
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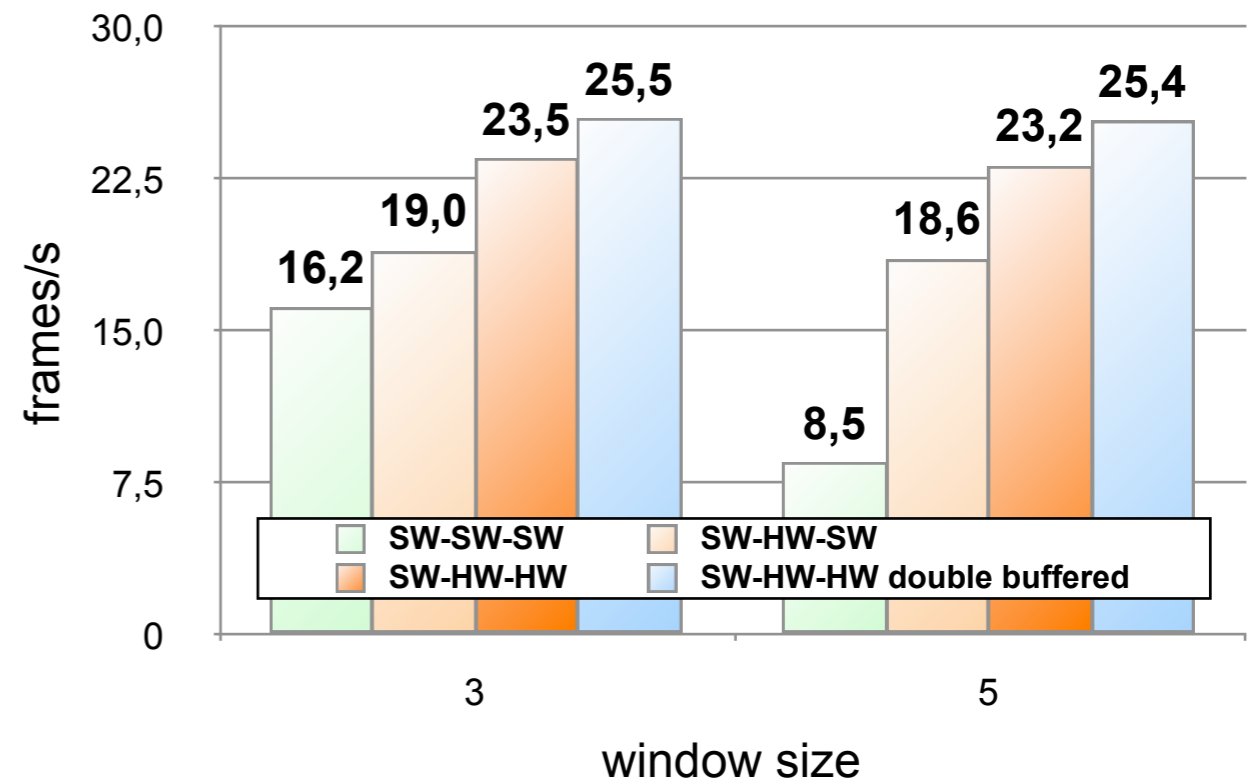
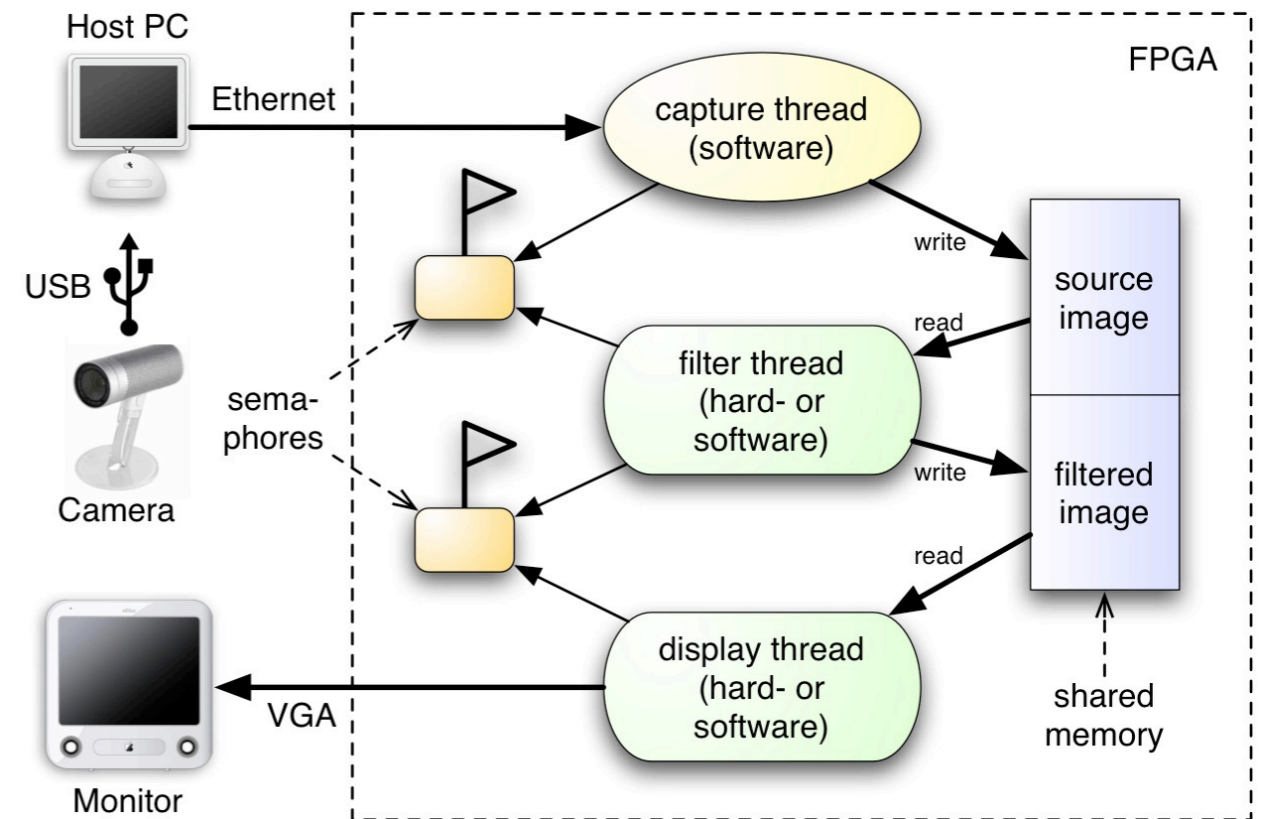
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 - u configures and builds static eCos library
- eCos extensions
 - u hardware thread object encapsulating delegate thread and OS interface “driver”
 - u profiling support to track the state of the hardware threads' OS synchronization state machines



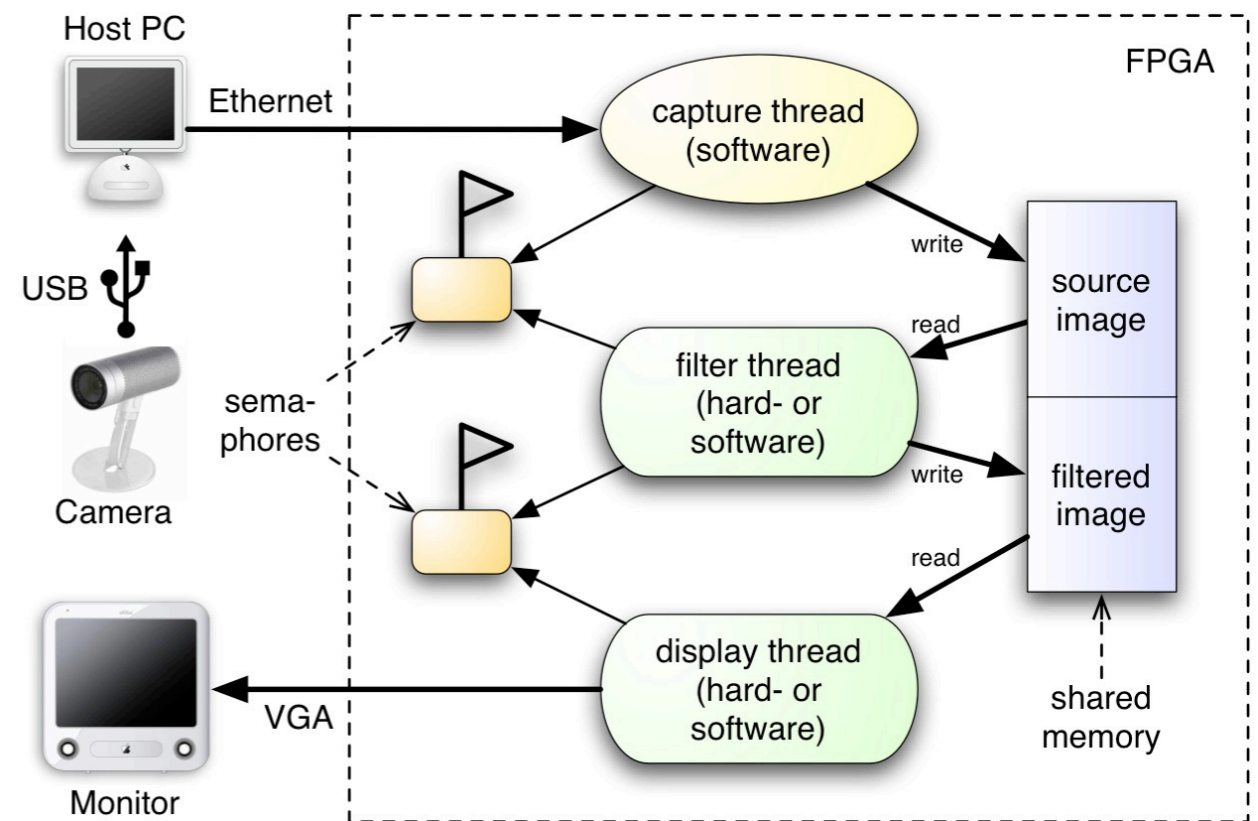
Case Study - Image Processing Filter

- three threads
 - capture image from Ethernet
 - apply LaPlacian filter
 - display image on VGA monitor
- threads communicate through shared memory
 - image resolution: 320x240 pixels, 8 bit greyscale
 - image data organized into blocks (e.g. 40 lines = 1 block)
 - a block is protected by two semaphores
 - “ready” semaphore: data can be safely written into this block
 - “new” semaphore: new data is available in this block



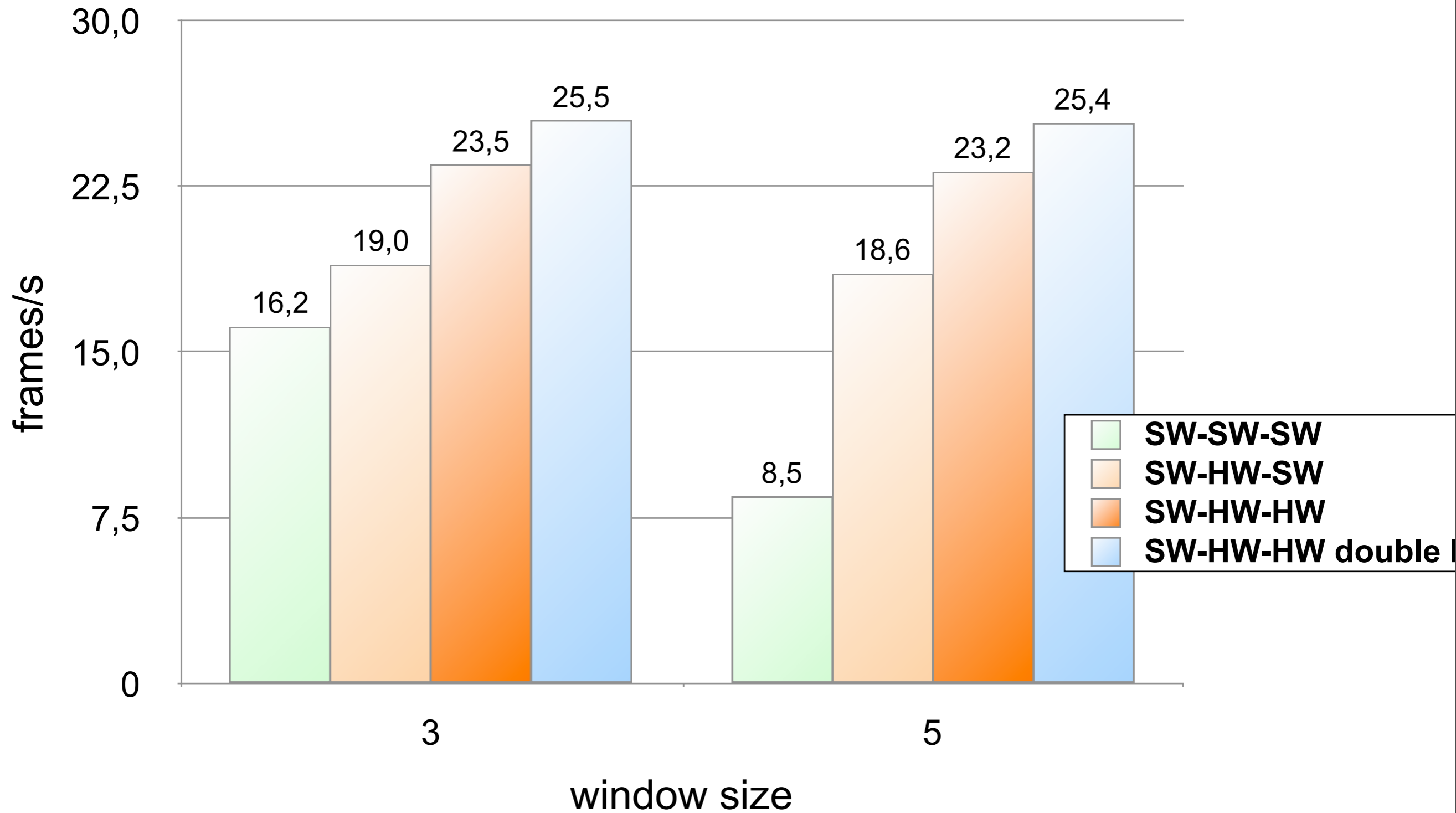
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SW-SW-SW	SW-HW-SW
SW-HW-HW	SW-HW-HW double buffered

Case Study - Results



Case Study - Results

-  **SW-SW-SW**
-  **SW-HW-SW**
-  **SW-HW-HW**
-  **SW-HW-HW double**